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SPACE AND DEFENSE SYSTEMS

FAIRCHILD SPACE AND DEFENSE SYSTEMS
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

FINAL REPORT
SOLID STATE HIGH RESOLUTION
MULTI-SPECTRAL IMAGER
CCD TEST PHASE

CONTRACT NO. NAS5-21597

for

National Aeronotics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland

1 May 1973

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Program Manager

Report No.
ED-AX-12

PREFACE

This report was prepared under National Aeronotics and Space Administration Contract No. NAS5-21597 for Goddard Space Flight Center, by Fairchild Space and Defense Systems, a division of Fairchild Camera and Instruments Corporation. The report covers work performed during the period from December 15, 1971 to April 30, 1973.

The program consisted of measuring the performance characteristics of charge coupled linear imaging devices, and followed a study, under the same contract, defining a multispectral imaging system employing advanced solid state photodetection techniques. The system study report, entitled FINAL REPORT, SOLID STATE HIGH RESOLUTION MULTI-SPECTRAL IMAGER was submitted to NASA on 16 July 1971.

ACKNOWLEDGEMENT

Fairchild Space and Defense Systems is indebted to NASA personnel for their valuable cooperation during the program. Special appreciation is expressed for the guidance and assistance provided by members of the Earth Sensors Branch of the Earth Observations Systems and Systems Engineering Division at Goddard Space Flight Center.

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SECTION 1

INTRODUCTION

1.1 GENERAL

The Space and Defense Systems Division of Fairchild Camera and Instruments is pleased to submit this final report in fulfilment of the CCD test phase of NASA Contract NAS5-21597, entitled Solid State Multi-Spectral Imager System.

The previous final report, summarizing the Phase I effort of this program, was submitted to NASA on 16 July 1971. That report concluded a study, analizing the use of solid state photodiode arrays in a Solid State Multi-Spectral Imager System for the Earth Resources Program.

This document summarizes the results achieved in testing charge coupled linear imaging devices. Specifically, it describes the test instrumentation, test procedures and test results obtained in characterizing 60 and 500 element Charge Coupled Linear Imaging Devices (CCLID) manufactured by Fairchild Camera and Instrument Corporation.

1.2 SUMMARY OF TEST RESULTS

Table 1-1 summarizes the test results achieved under this program, and compares them with the characteristics of the Fairchild self scanned photodiode arrays reported in the first final report dated 16 July 1971.

The element to element pitch of the CCLID is 20% larger than that of the photodiode array (BLA) but the number of elements per chip in the CCLID is twice that of the BLA. New developments at Fairchild will result with CCLID's with 1000 and 1500 elements per chip, 4 to 6 times the BLA elements.

The CCLID has an on-chip amplifier which delivers a signal as large as 600mV at saturation. BLA signal could not be detected without a fairly sophisticated off-chip amplifier.

The CCLID clocking structure is 3 phase, compared with the simpler 2 phase BLA structure. The charge transfer process in CCD's causes some signal to be left behind (Charge Transfer Inefficiency).

TABLE 1-1

SUMMARY OF TEST RESULTS

Parameter	CCLID 500	Photodiode Array
Element Pitch	0.0012"	0.001"
Elements/Chip	500	128 (256 on later units
On-Chip Amplifier	Yes	No
Clocking Structure	3 Phase	2 Phase
Charge Transfer Efficiency	>0.9999	N/A
Uniformity at Dark	± 1.5% Sat	± 3.4% Sat.
Uniformity at Near Saturation	± 12.5% Sat	± 9.1% Sat.
Linearity	$\gamma = 0.96$	$\gamma = 1$ (projected)
Min. Detectable Irradiance, 2850°K	1.02 $\mu J/M^2$	2.52 $\mu J/M^2$ (measured 1.26 $\mu J/M^2$ (projected
Saturation Irradiance, 2850°K	1134 $\mu J/M^2$	155.4 $\mu J/M^2$
Dynamic Range	1100:1	70:1 (measured) 1050:1 (projected)
Peak Spectral Responsivity at Chip Output	3.6 $mV/uW/cm^2$	Not Measured
Crosstalk $\lambda < 0.67$ um	1%	Not Measured
Crosstalk $\lambda > 0.67$ um	10%	Not Measured
Temperature Effects	Small Change in γ	Not Measured
Dark Signal	0.4 % Sat.	28.6% Sat.
Maximum Clocking Rate	2MHz	200 KHz

In the CCLID-500 the charge transfer efficiency is better than 99.99% per transfer at high signal levels. However, the BLA suffers a loss of signal through a capacitive division between the photojunction (0.13pf) capacity and the on-chip multiplexing bus capacity (8.7pf). As a result, the amplitude at the BLA output is only 2% of the photojunction signal.

At dark, the CCLID non uniformity is 1.5% of saturation compared with 3.4% non uniformity of the BLA. At near saturation, the BLA uniformity is slightly better than that of the CCLID. During current work, under Naval Electronics Systems Command (NESC) Contract No. N00039-73-0015, the CCLID-500 package was improved, to eliminate the need for opaquing the bulk silicon of the array. Uniformity tests on the new package showed an average of 6% highlight non uniformity compared with the BLA's 9.1%.

The signal transfer curve of the CCLID shows a gamma of 0.96. BLA linearity was not tested, but was calculated to have a gamma of unity.

The minimum detectable irradiance of the CCLID is about half that of the BLA. Its dynamic range is about equal to the BLA's projected dynamic range (1100:1), and 15 times better than the BLA's measured dynamic range. During the NESC program mentioned above, CCLID's operated at higher clock voltages showed an average dynamic range of 4100:1.

CCLID element to element crosstalk was found to be 1% at the shorter wavelengths and 10% at the longer wavelength. This test was not performed on the BLA.

Temperature tests on the CCLID showed a small increase in gamma with temperature. The BLA was not tested under temperature changes.

The CCLID's dark signal at room temperature measured to be about 0.4% of saturation, while the BLA's dark signal was 28.6% of saturation.

The maximum clocking frequency of the BLA was 200KHz while that of the CCLID was 2MHz. New CCLID's are designed to operate at 5-10MHz.

1.3 CONCLUSIONS

The performance of the charge coupled linear imaging devices tested under this program proves that the charge coupled device technology has passed the exploratory stage and is now indeed a technology capable of producing viable electro optical sensors for most applications.

The CCLID was found to have equal or better performance characteristics when compared to the BLA. Fairchild's recent development of longer CCLID's charge coupled area imaging devices, and anti blooming and exposure control features (see Section 7) opens the door for new sensor configurations designed especially for multi-spectral imaging applications. Such sensors could take the form of several long CCLID's on one chip, where each CCLID will operate at a different spectral band.

1.4 OUTLINE OF REPORT

The remaining sections of this report contain the information listed below:

Section 2

Description of the CCLID-60 and CCLID-500 tested under this program.

Section 3

A listing of the tests performed on the CCLID's.

Section 4

Description of the test setup and its components.

Section 5

A description of the calibration of the test setup and the procedures used in testing the CCLID's.

Section 6

Details of the test result.

Section 7

A brief description of Fairchild's new developments in charge coupled imaging devices.

Appendix A

An introduction to charge coupled device theory and operation.

SECTION 2

THE CHARGE COUPLED LINEAR IMAGING DEVICE

2.1 GENERAL

Two types of charge coupled linear imaging devices (CCLID) were evaluated under this program - 60 element CCLID's and 500 element CCLID's. This section describes the structure and operation of these specific devices. A general discussion of charge coupled device theory appears in appendix A. Section 7 describes other types of charge coupled devices which are currently under development at Fairchild Camera and Instrument Corporation.

2.2 CCLID STRUCTURE

The CCLID 60 and CCLID 500 are more than a photosensitive charge coupled shift register - they are a complex system containing an imaging section, a charge transport section and a preamplifier, all on one monolithic silicon chip. Both devices are of identical construction except for the number of photoelements. The CCLID 60 contains 60 photoelements and CCLID 500 contains 500 photoelements. Both CCLID's are three phase buried N channel devices. Each photoelement is 1.2 mil square.

Figure 2-1 shows the structure of a CCLID chip. The photoelements comprise a linear array in the center of the chip. The individual elements are separated from each other by a channel stop of a serpentine construction. The channel stop surrounds each photoelement on three sides, thus enabling the transfer of charges accumulated in the photoelement only through the unobstructed side. This design enables the use of a common electrode (photogate) for all photoelements. Similarly, a common transfer gate can be used for transferring the accumulated photocharges from the photoelements to the transport registers. The photogate is constructed of polysilicon, which is basically transparent to wavelengths within the silicon sensitive range. (See Figure 6-14. The transparent gate causes the sharp cutoff at .4 μm).

An examination of the diagram in figure 2-1 shows that the serpentine channel stop forces the charges from adjacent photoelements to be transferred in opposite directions into two vertical transport registers. This design was chosen for two reasons:

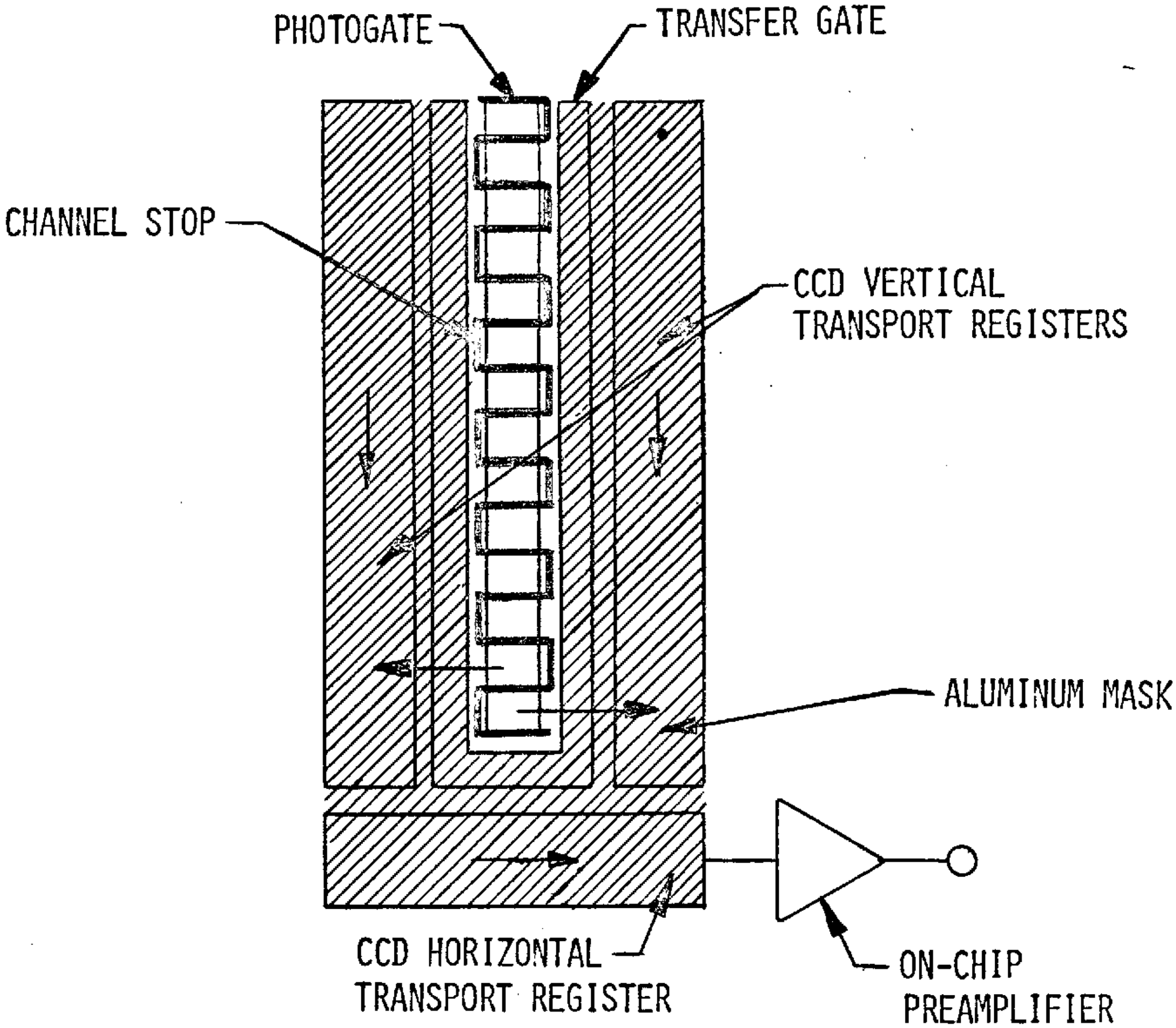


FIGURE 2-1 CCD LINEAR IMAGING DEVICE

a) The transport register requires three cells for each photoelement. By using two registers, the pitch of the transport register cells is doubled (2/3 of that of the photoelement instead of 1/3). This enabled to maintain the photoelements at a 1.2 mil pitch without changing the existing proven design rules.

b) The transfer frequency and the number of transfers in each of the vertical transport registers is halved, thus improving the total transfer efficiency of the CCLID.

The use of two vertical transport registers, however creates an added complexity- the need for a horizontal transport register. This register serves as a video combining register. It accepts the signals from both vertical registers simultaneously, and forwards them to the preamplifier in succession thus recombining the two interlaced video streams back into one.

As seen in figure 2-1, the transport registers, both horizontal and vertical, are masked by a layer of aluminum, thus preventing the generation of photocurrents within the transport registers. Since the bulk silicon outside of the CCLID's active area can also contribute spurious photocurrent through leakage into the transport registers, the exposed inactive area of the CCLID, as well as the on-chip preamplifier, are covered by opaque paint after the chip is mounted on the header.

Figures 2-2 and 2-3 are photomicrographs of a CCLID 60 and CCLID 500 respectively. Figure 2-2 is taken at a higher magnification and clearly shows the serpentine structure of the photoline, the electrodes and access busses of the transport registers and the aluminum mask.

2.3 CCLID OPERATION

The charges in the CCLID cells are transported by applying clocks to the CCD electrodes in the proper sequence. Figure 2-4 is a schematic diagram of the CCLID-500, and shows the direction of charge flow from the photoelements to the output preamplifier.

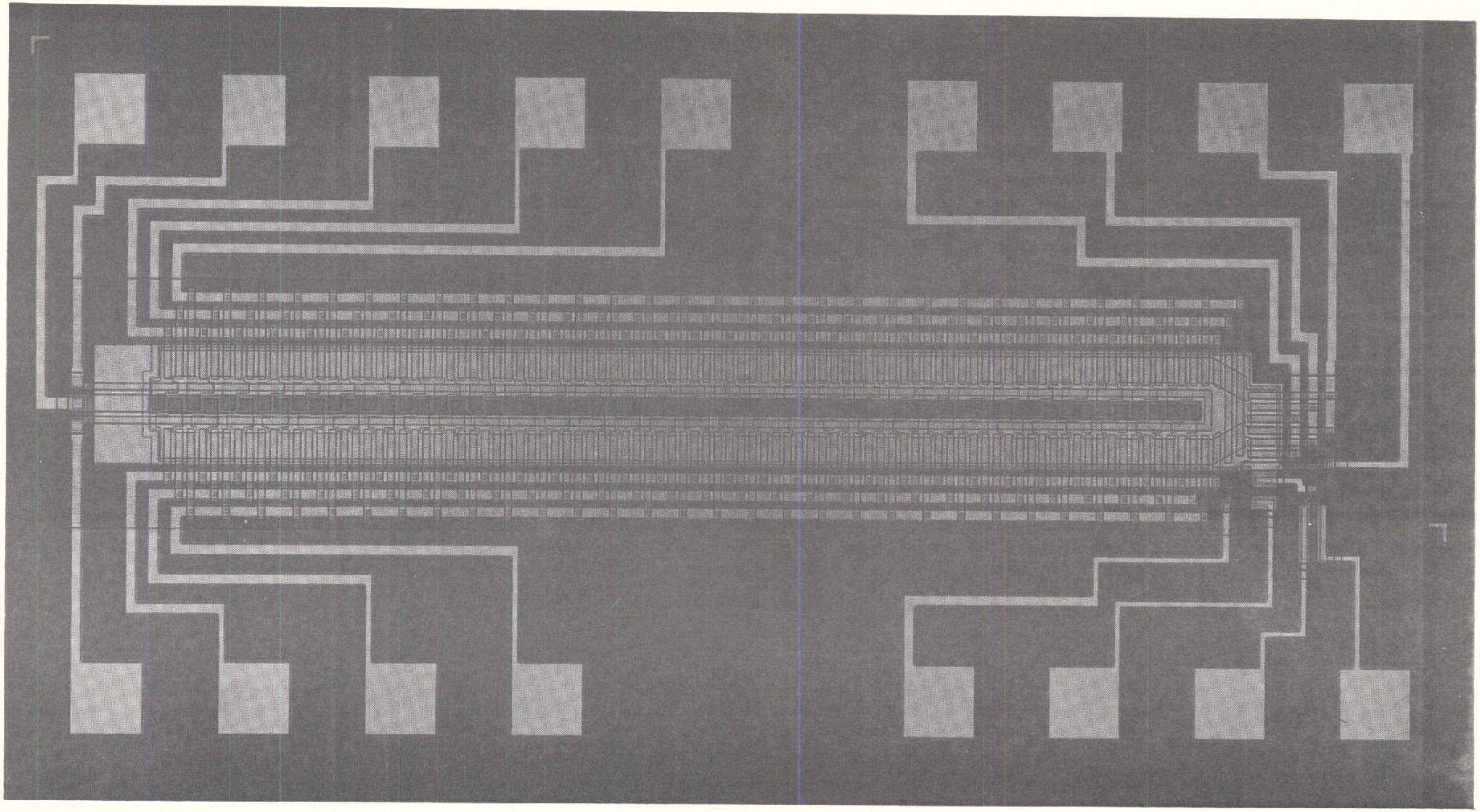


FIGURE 2-2. PHOTOGRAPH OF CCLID-60

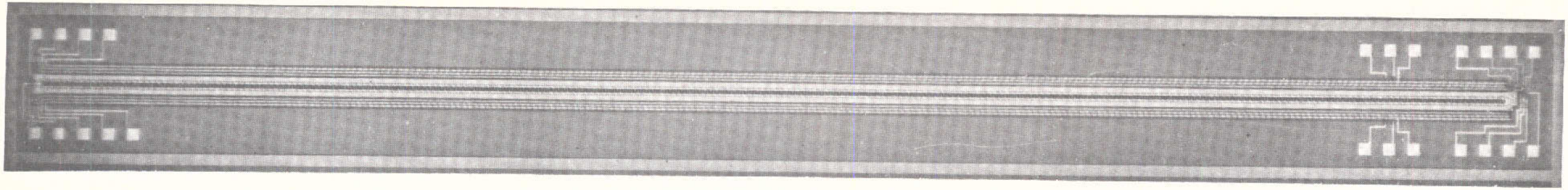


FIGURE 2-3. PHOTOGRAPH OF CCLID-500

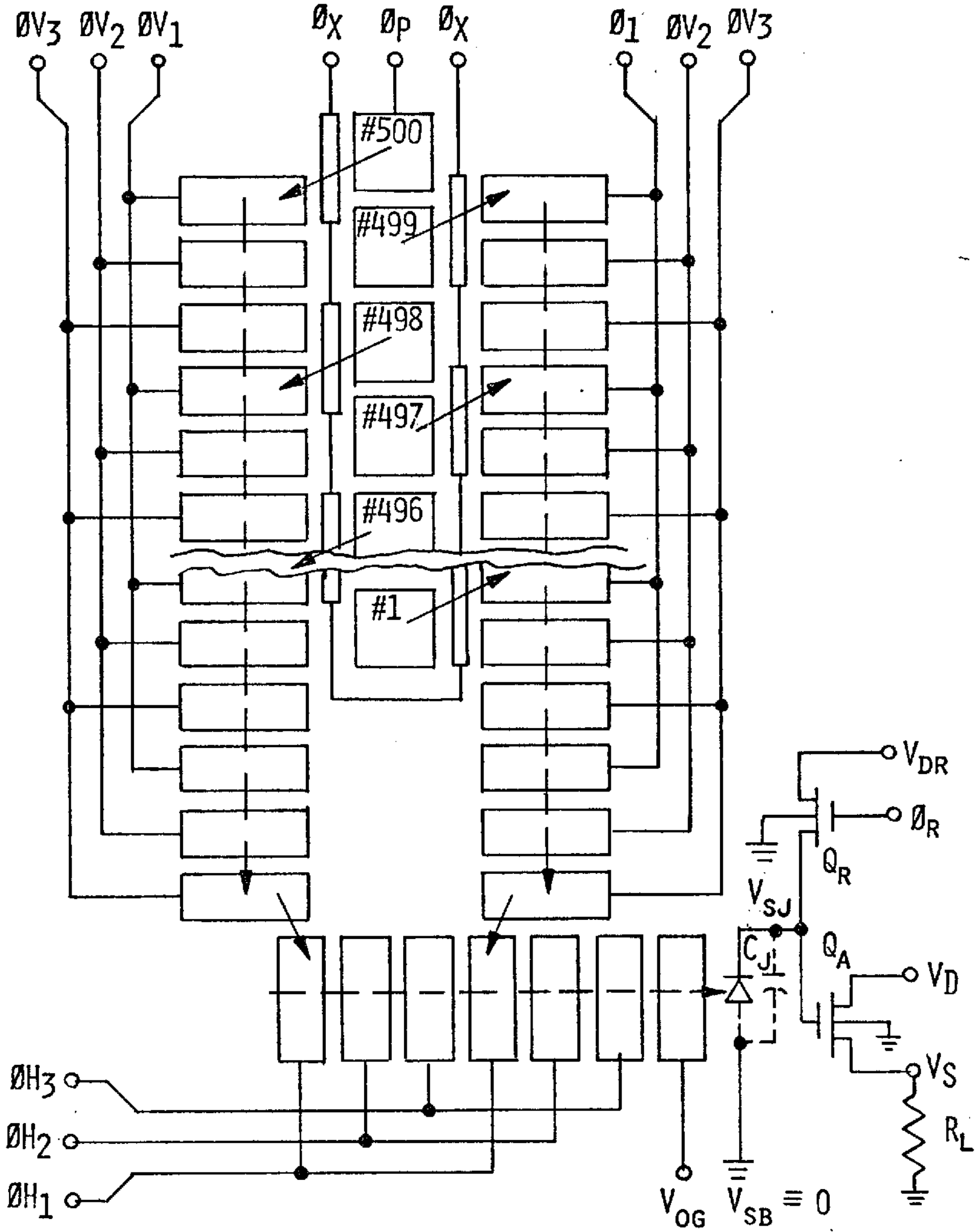


FIGURE 2-4

CCLID-500 CIRCUIT SCHEMATIC

One CCLID cycle consists of the following sequence of functions:

a) A parallel charge transfer from the photoelements to both odd and even vertical transport registers.

b) A series of transfers, transporting the video down the vertical registers and into the horizontal register.

c) Horizontal transfers and recombination of the vertical registers data into one video stream.

d) Charge to voltage conversion in the on-chip preamplifier.

Figure 2-5 shows the timing diagram for the CCLID. The line integration time (t_I) consists of one full period of the parallel transfer pulse (ϕ_p). The direction of charge flow in the CCLID is from a low electrode potential (shallow well) to a high electrode potential (deep well).

The parallel charge transfer from the photoelements to the vertical transport registers occurs when ϕ_p goes low. During this period, the vertical registers are not clocked. Instead, ϕV_1 is kept at a high potential, allowing the charge to move from the photoelements into the first cell of their corresponding 3-cell register structure. Since ϕV_2 and ϕV_3 are at a low potential, the photocharge will remain under the cells controlled by the ϕV_1 electrode until the end of the parallel transfer. The parallel transfer gate ϕ_X is used to allow charge transfer during the parallel transfer period and to block charge leakage (enable light current integration) from the photoelements during the remainder of the integration time. The recommended parallel transfer period tx is 40 us or longer.

At the end of the parallel transfer, the vertical registers are clocked at half the video element rate, and the horizontal register at the full video element rate. When ϕV_1 is low and ϕV_2 high, charge is transferred from the first to the second cell of each register element structure. The transfer from the second to the third cell occurs when ϕV_2 is low and ϕV_3 is high. When ϕV_3 is low and ϕV_1 high, the charge is transferred from the third cell of one register element to the first cell of the next register element.

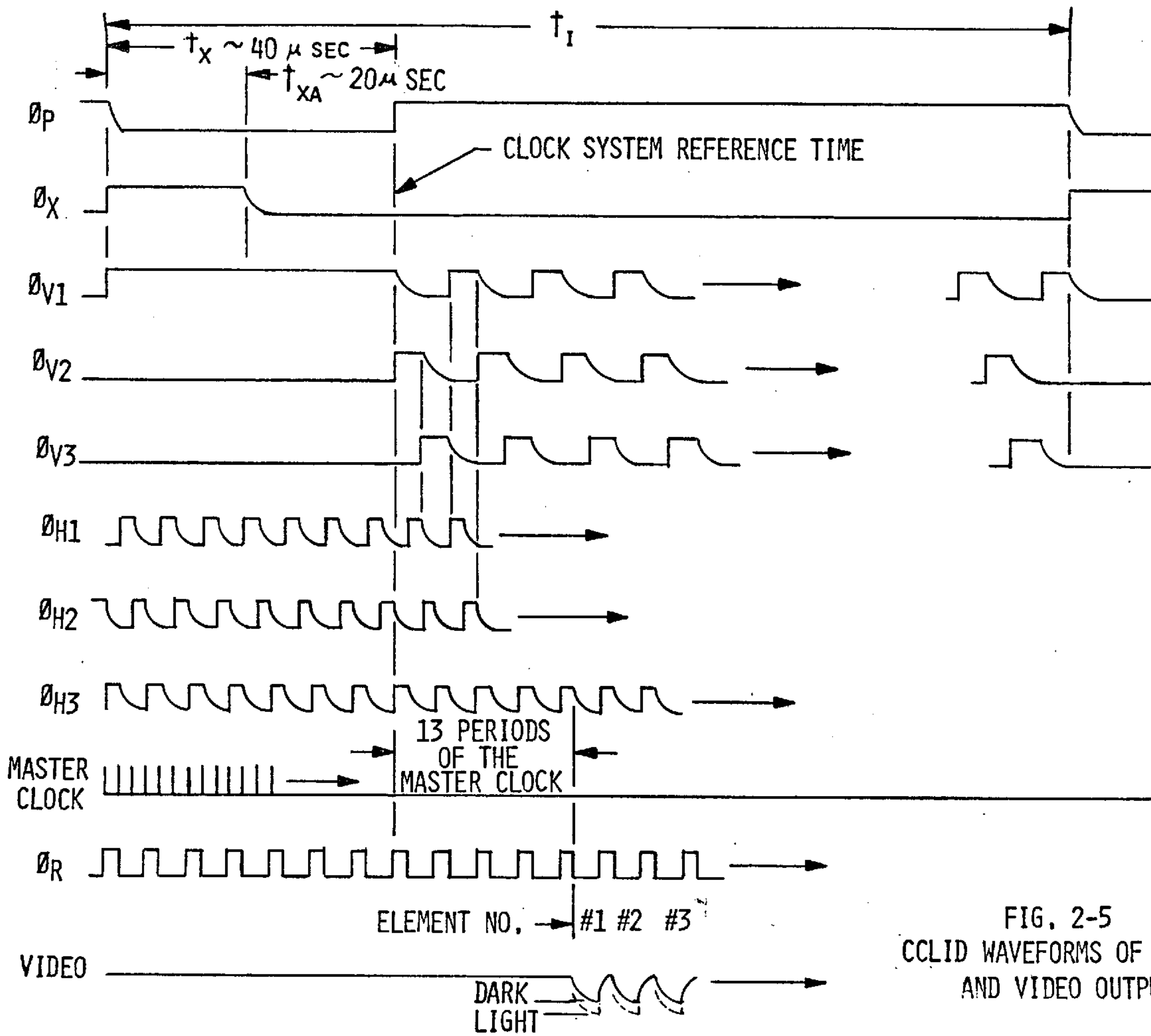


FIG. 2-5
CCLID WAVEFORMS OF CLOCKS AND VIDEO OUTPUT

At the same time (ϕV_3 goes low), the horizontal clock ϕH_1 goes high, and the charge content of the end cells in both vertical registers is transferred to two adjacent first cells in the horizontal registers. ϕH_1, ϕH_2, and ϕH_3 transport these charges along the horizontal (combining) register toward the on-chip output preamplifier.

The falling edge of $\phi H3$ transports the charge past an output gate (V_{OG}) into a charge detector. The charge detector is a junction capacitor (C_j) in a form of a back biased diode. The threshold voltage on the output gate is adjustable and set for best array performance.

The on-chip preamplifier is a resettable MOS source follower. The charge transferred into C_j generates a voltage V_{sj} at the gate of the source follower Q_A. A proportional voltage V_s appears across the external load resistor R_L at the source of Q_A. The capacitor C_j is rechraged once per element transfer as the reset MOS, Q_R, is momentarily turned on with the positive reset pulse, ϕ_R. ϕ_R is shorter than ϕH_3, and occurs within the period in which ϕH_3 is high. The resulting video signal at V_s is a pulsed video, going negative with increased light signal and resetting to a reference level at the end of each array element signal.

As shown in the timing diagram, the falling edges of the CCLID clocks are sloped. The pulse slopes can be adjusted to peak the transfer efficiency of the device. ϕ_p and ϕ_x do not require a slope. ϕ_R is not a CCD pulse, and should have sharp transitions.

2.4 CCLID INTERFACE

Both CCLID-500 and CCLID 60 are mounted on a ceramic 24 pin dual-in-line package, under a protective cover with a glass window (see figure 2-6). The package size is 1,280" x 0.600". Mating 24 pin DIP sockets are commercially available from several sources, both with cam-operated contacts for multiple insertions and fixed contacts for semi permanent installation.

The CCLID will operate at a wide range of input signal levels. High frequency operation requires higher voltages than low frequency. The maximum operating frequency of the CCLID is 2 MHz.

Table 2-1 lists the pin connections and Table 2-2 the input signal requirements for the CCLID.

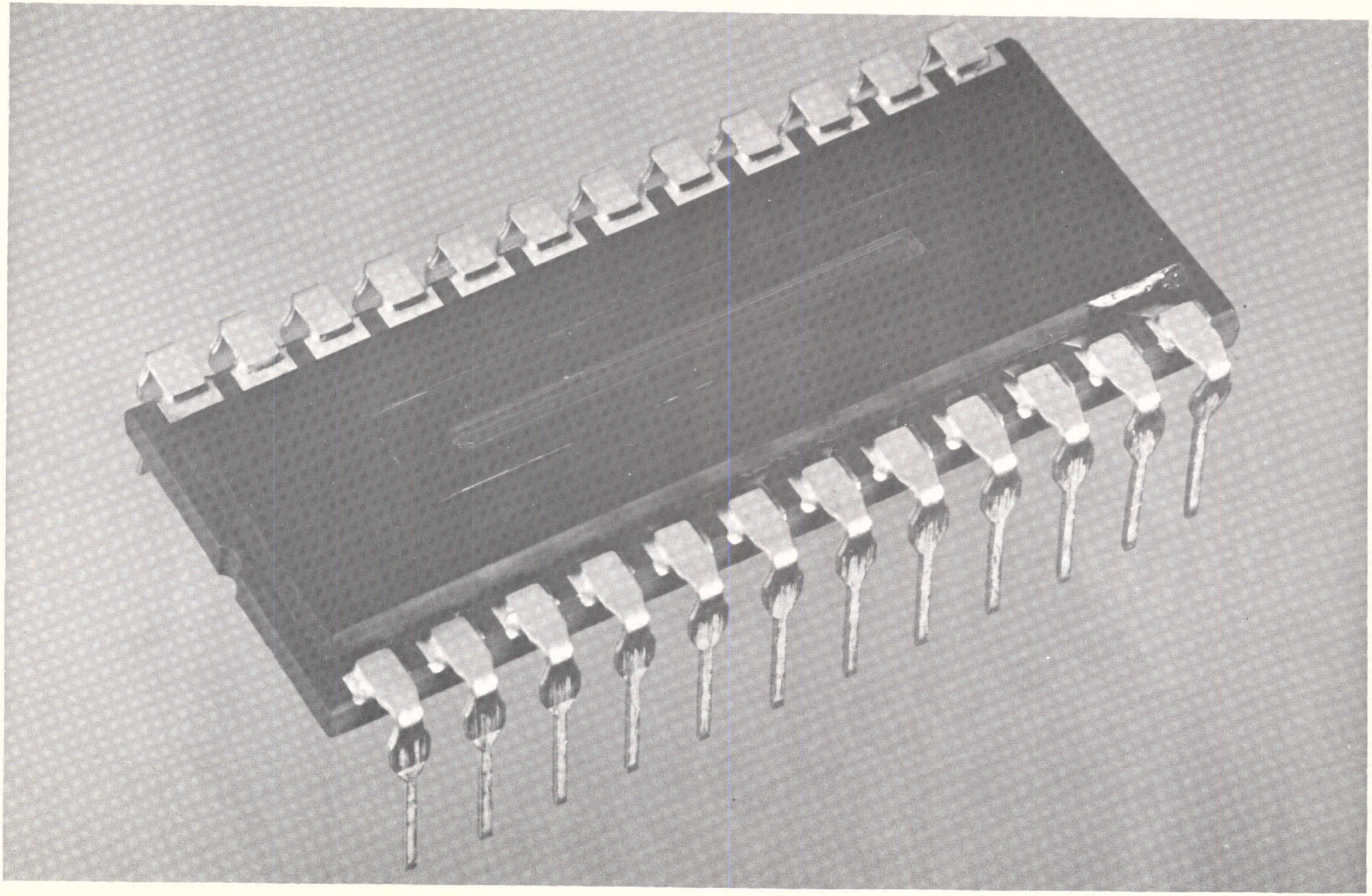


FIGURE 2-6. PACKAGED CCLID-500A

TABLE 2-1

CCLID PIN CONNECTIONS

PIN #	SIGNAL NAME	DESCRIPTION
1	ϕ_p	Parallel Transfer Pulse
2	ϕ_x	Parallel Transfer Gate Pulse
3	ϕ_{V1}	Phase 1 Clock, Vertical Registers
4	ϕ_{V2}	Phase 2 Clock, Vertical Registers
5	ϕ_{V3}	Phase 3 Clock, Vertical Registers
6	ϕ_{V1}	See Pin 3
7	ϕ_{V2}	See Pin 4
8	ϕ_{V3}	See Pin 5
9	ϕH_3	Phase 3, Horizontal Register
10	ϕH_2	Phase 2, Horizontal Register
11	ϕH_1	Phase 1, Horizontal Register
12	V_{OG}	Output Gate Bias
13	V_s	Output Video Signal
14	V_{DD}	On-Chip Preamplifier Drain Voltage
15	V_{DR}	Reset MOS Drain Voltage
16	ϕ_R	Reset Pulse
17	ϕ_{V3}	See Pin 5

TABLE 2-1
(cont'd)

PIN #	SIGNAL NAME	DESCRIPTION
18	ϕ_{V2}	See Pin 4
19	ϕ_{V1}	See Pin 3
20	ϕ_{V3}	See Pin 5
21	ϕ_{V2}	See Pin 4
22	ϕ_{V1}	See Pin 3
23	ϕ_{x}	See Pin 2
24	GND	Substrate Ground

TABLE 2-2

INPUT SIGNAL REQUIREMENTS

SIGNAL DESCRIPTION	PULSE SWING (V) LOW	PULSE SWING (V) HIGH	D.C. LEVEL (V)
CCD CLOCKS	-2 to 0	3.5 to 9	
RESET CLOCK	0 to +2	5 to 9	
PREAMP DRAIN		12 to 18	12 to 18
RESET DRAIN			12 to 18
OUTPUT GATE BIAS			0 to 2
GROUND			0

SECTION 3

TEST PLAN

3.1 GENERAL

The CCLID test plan called for the evaluation of one or more CCLID-60, two or more CCLID-500 arrays, and the construction of electronics to operate the photo-array and a data collection system.

The CCLID-60 and CCLID-500 test samples have been produced under a Fairchild internal development program. These are not deliverable, and their development and fabrication costs are not included in the cost of the test program.

The major components of the test setup are existing Fairchild capital equipments. These too are not deliverable, and their cost is not included in the cost of the program.

3.2 CCLID TESTS

Table 3-1 lists the tests performed during this program and the information derived from these tests. The test procedures and analysis of test results appear in sections 5 and 6 of this report,

The CCLID transfer characteristics were measured with an automated data collection system, which recorded the test data on magnetic tape. The test data was then processed and reduced by a computer. Data for other tests was taken manually, using an oscilloscope as the principal measuring instrument.

TABLE 3-1

CCLID TESTS

	TEST DESCRIPTION	DERIVED INFORMATION
1.	Charge Transfer Efficiency	Charge Transfer Efficiency
2.	Transfer Characteristics	Dark Signature, Uniformity Linearity of response
3.	Noise Characteristics	Sensitivity, Dynamic Range
4.	Spectral Response	Spectral Response Curve
5.	Crosstalk	Crosstalk and Element Profile at different wavelengths.
6.	Temperature	Variation of response with temperature
7.	Dark Current	Array output at dark

SECTION 4

TEST SETUP

4.1 GENERAL

The CCLID test setup is a modular system designed to fully characterize the arrays with minimal setup changes. The test can be performed manually or automatically. Optical and mechanical conditions are changed by addition, removal or substitution of interchangeable modules. Electrical conditions are changed mostly by control switches. In the automatic mode, the test data is processed by a computer. The computer programs, therefore, are as much a part of the setup as the test hardware.

This section describes the test setup, its components and its application for various tests.

4.2 TEST SETUP DESCRIPTION

The CCLID test setup includes the following subsystems: Optical bench and light tight enclosure, calibrated light source, optical filters, array controller and amplifier(excerciser),automatic test console, manual monitoring equipment and a light probe.
Figure 4-1 is a block diagram of the linear CCLID test setup. Figure 4-2 is a photograph of the optical bench and enclosure, the light source, neuteral density filter, and the X-Y stage holding the CCLID and excerciser. Figure 4-3 is a photograph of the light probe.

4.2.1 Optical Bench and Enclosure

The optical bench is 2 meters long, Beck model 22-965 precision lathe bed. Its dovetailed mounting surface is designed to accept snap-on equipment carriers made by Ealing Inc. The bench is enclosed by a light tight enclosure. The enclosure is divided into two compartments separated by a partition. One compartment contains the light source and the other contains the optical modules, CCLID excerciser and CCLID under test. An opening in the partition allows the light to reach the array through a diffusing plate.

TABLE 4-1

CENTER WAVELENGTHS OF NARROWBAND FILTERS

FILTER #	λ_c (um)
1	0.4047
2	0.4861
3	0.5893
4	0.6708
5	0.7670
6	0.9000
7	1.014
8	1.1
9	1.2

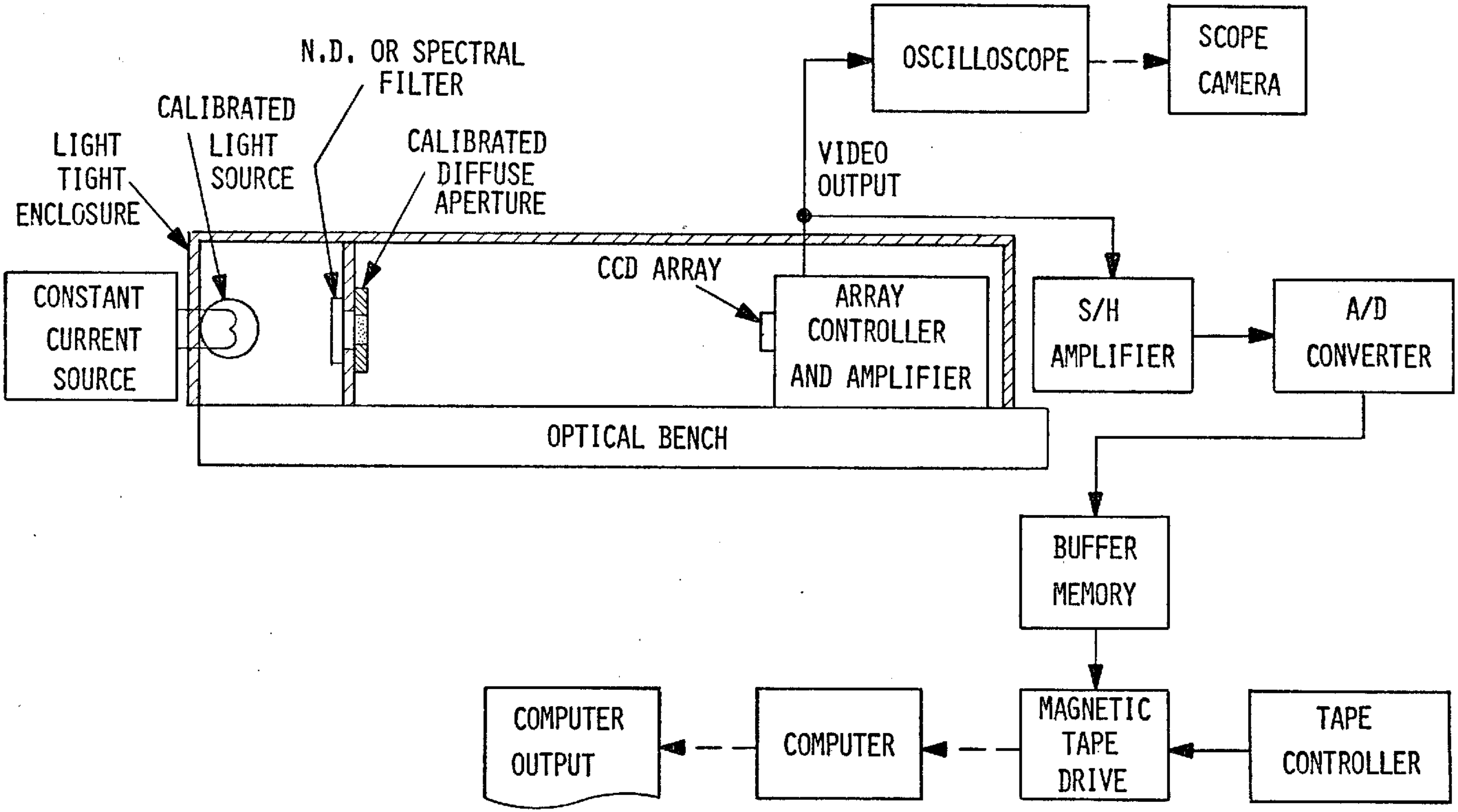


FIGURE 4-1 INSTRUMENTATION FOR LINEAR CCI TESTS

4.2.2 Calibrated Light Source for the Optical Bench

The light source is a 1000 watt tungsten halogen lamp controlled by a constant current supply. The lamp housing and constant current supply are made by EG&G.

An EG&G 580/585 spectro radiometer system is used to calibrate the light source color temperature. The calibration was performed with a diffuse aperture in front of the light source. The lamp current was 7.1 amperes and the spectro radiometer was placed 142.75 cm away from the aperture. A similar measurement was taken of the light source without the diffused aperture. Figure 4-4 shows the measured spectral content of the diffused light. Figure 4-5 shows the spectral content of the undiffused light source. Figure 4-6 is a photograph of the light source calibration setup and includes the optical bench setup with the spectroradiometer mounted in it.

4.2.3 Optical Filters

A series of optical filters were used during the CCLID tests, both for broadband and narrowband attenuation.

4.2.3.1 Neuteral Density Filters

Neuteral density filters were used for broadband light source attenuation during the transfer characteristics test. The two filters used had nominal densities of 1.0 and 2.0 and were flat within the silicon bandwidth. Figures 4-7 and 4-8 show the transmission characteristics of the N.D. 1.0 and N.D. 2.0 filters used in this test.

The neuteral density filters provided coarse light intensity steps. Finer adjustment of light intensity was achieved by varying the distance between the light source and the CCLID under test.

4.2.3.2 Narrow Band Filters

The narrowband filters were used in the generation of the CCLID spectral response curve. Each filter has a bandwidth of approximately 10 nm. Table 4-1 lists the center bandwidths of the filters used, and figures 4-9 through 4-17 show their transmission characteristics.

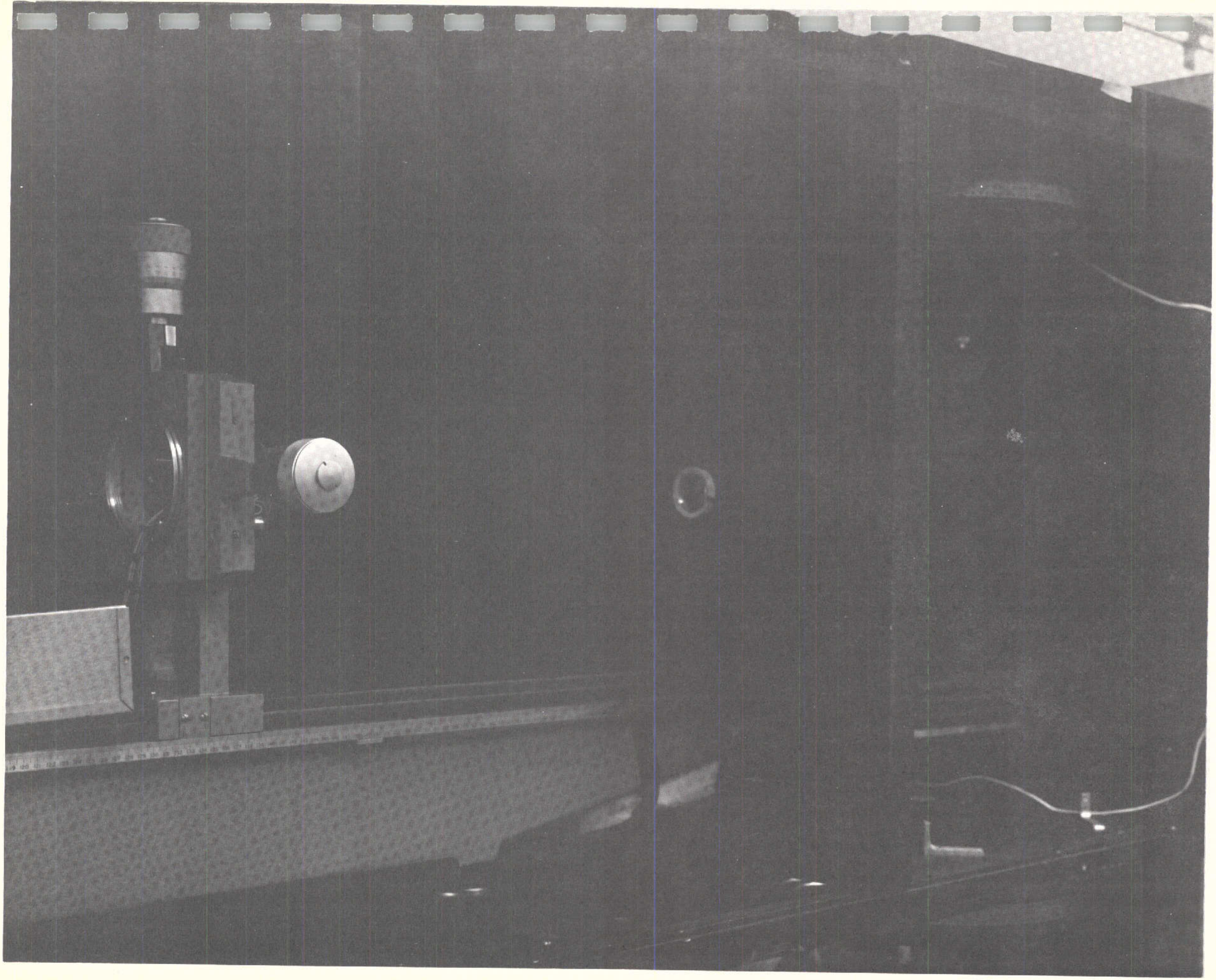


FIGURE 4-2. OPTICAL BENCH AND ENCLOSURE

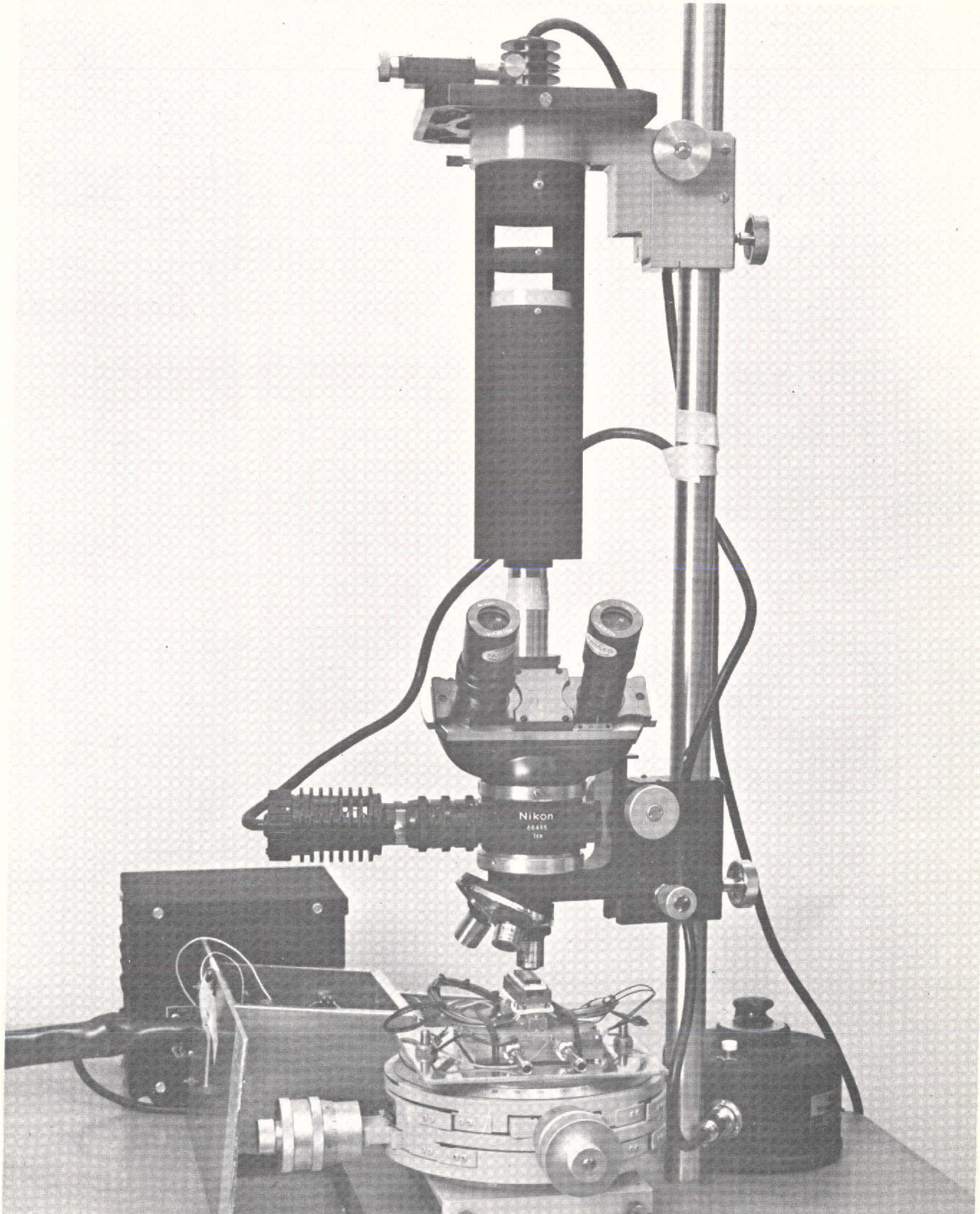


FIGURE 4-3. LIGHT PROBE

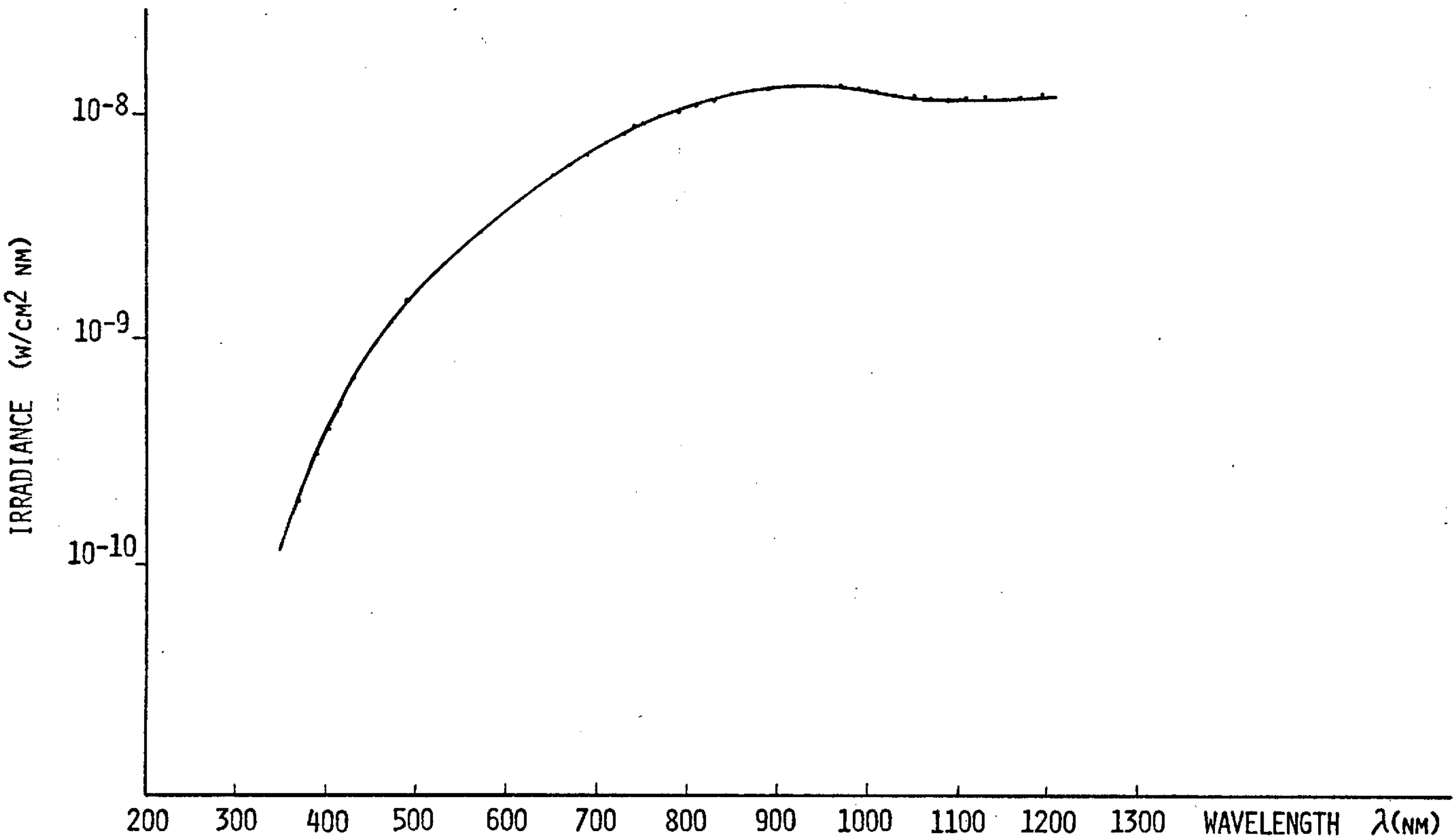


FIGURE 4-4 DIFFUSED LIGHT SOURCE CALIBRATION

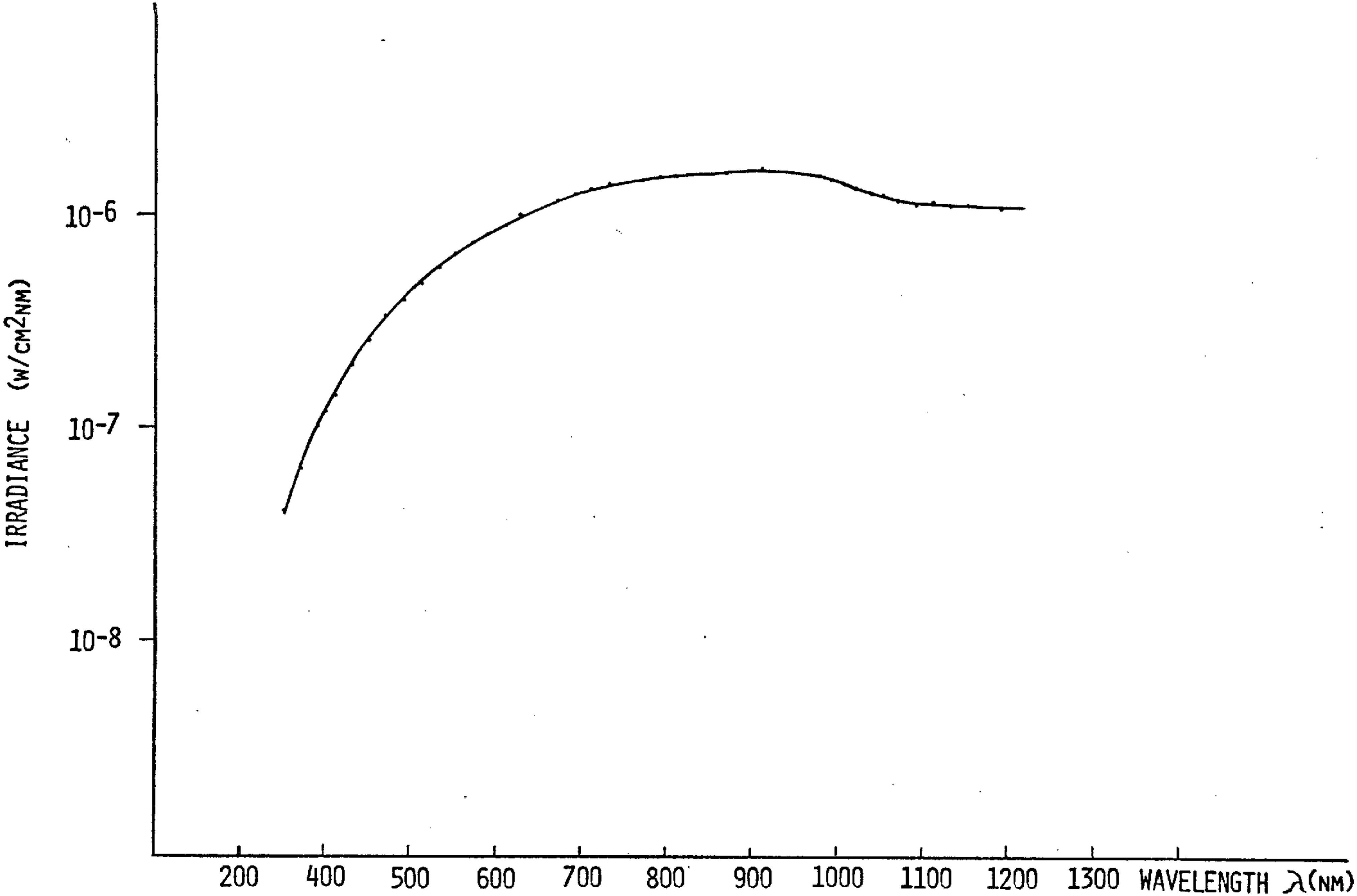


FIGURE 4-5 UNDIFFUSED LIGHT SOURCE CALIBRATION

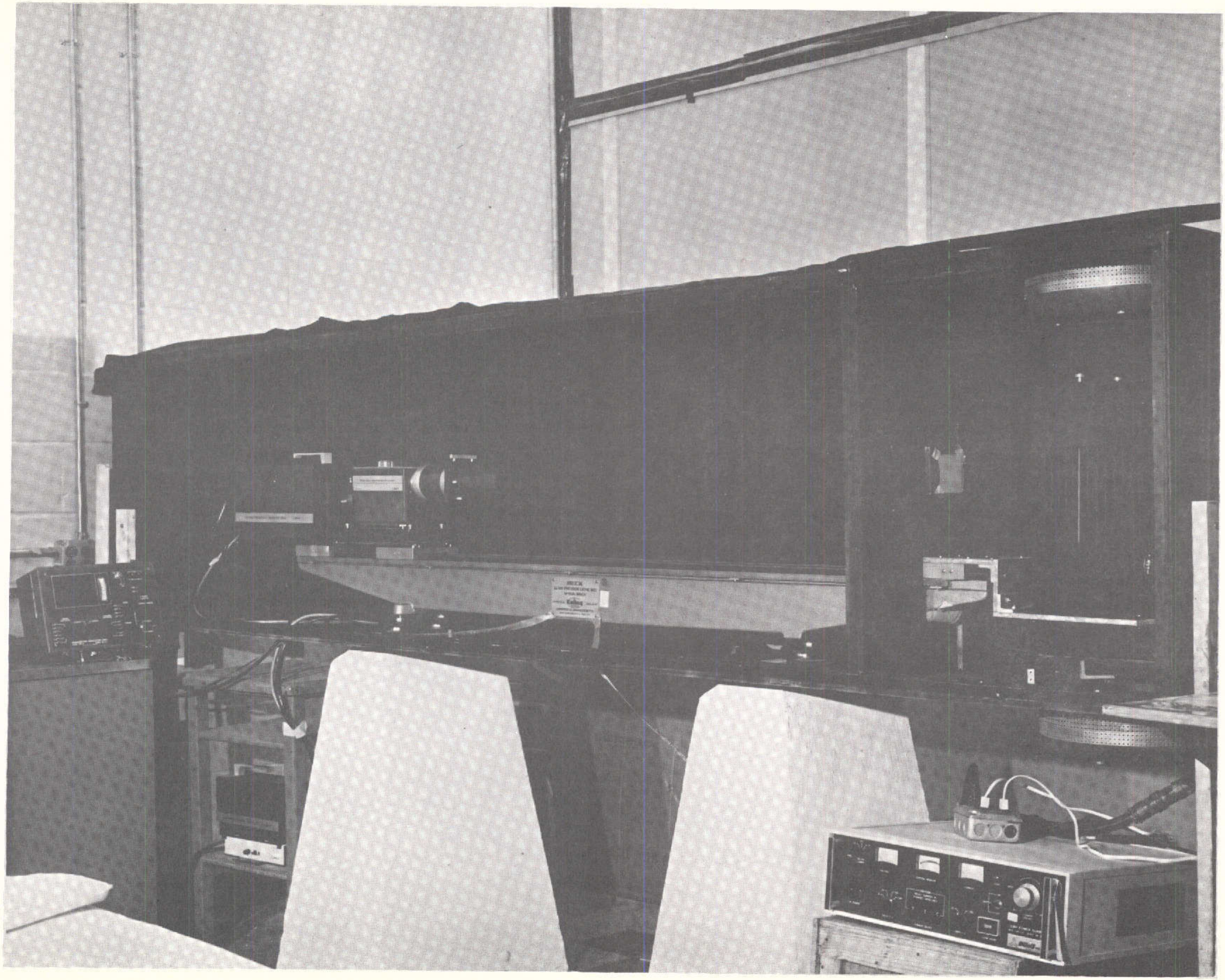


FIGURE 4-6. LIGHT SOURCE CALIBRATION SETUP

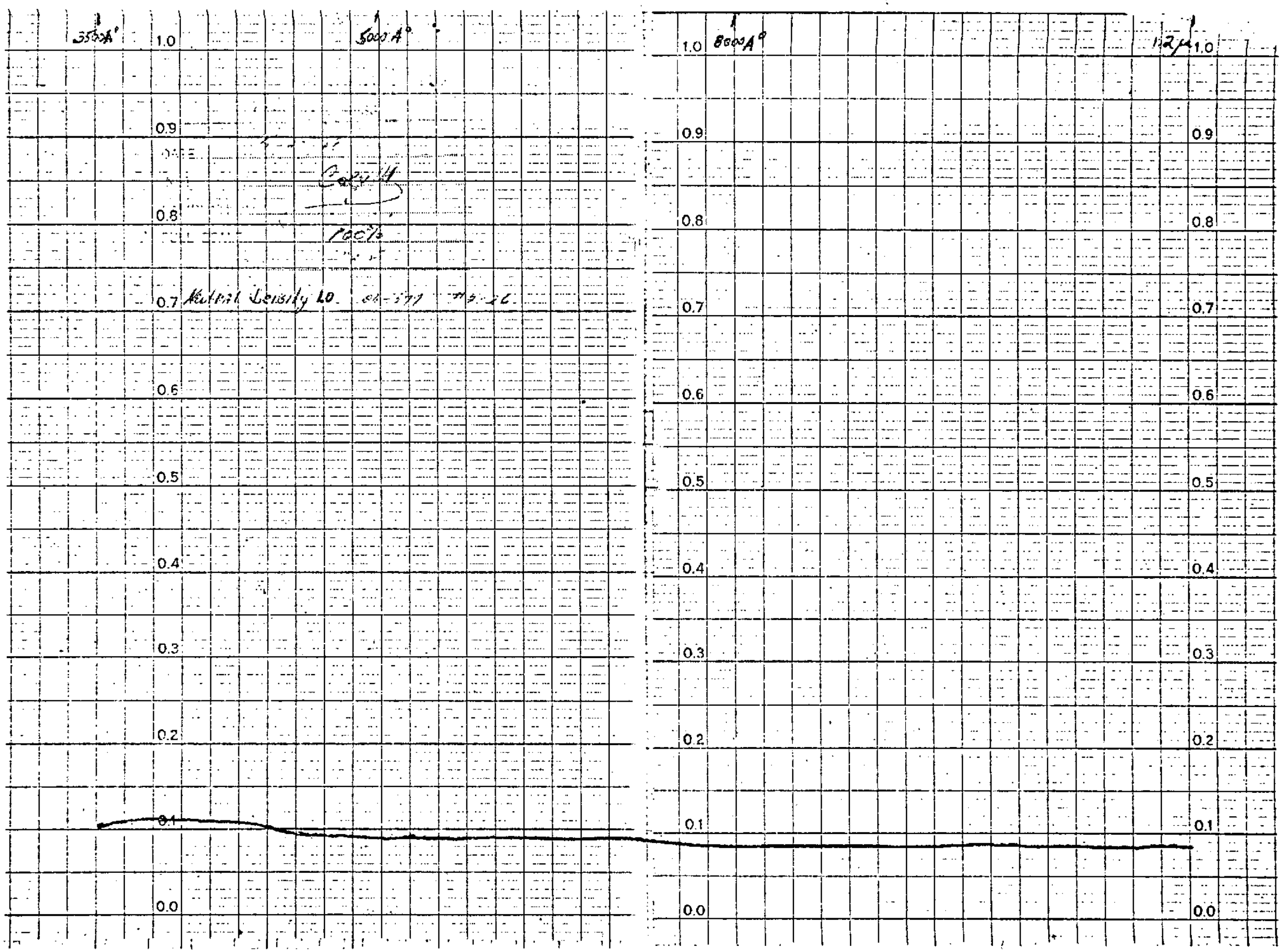


FIGURE 4-7 N.D.1.0 FILTER CURVE

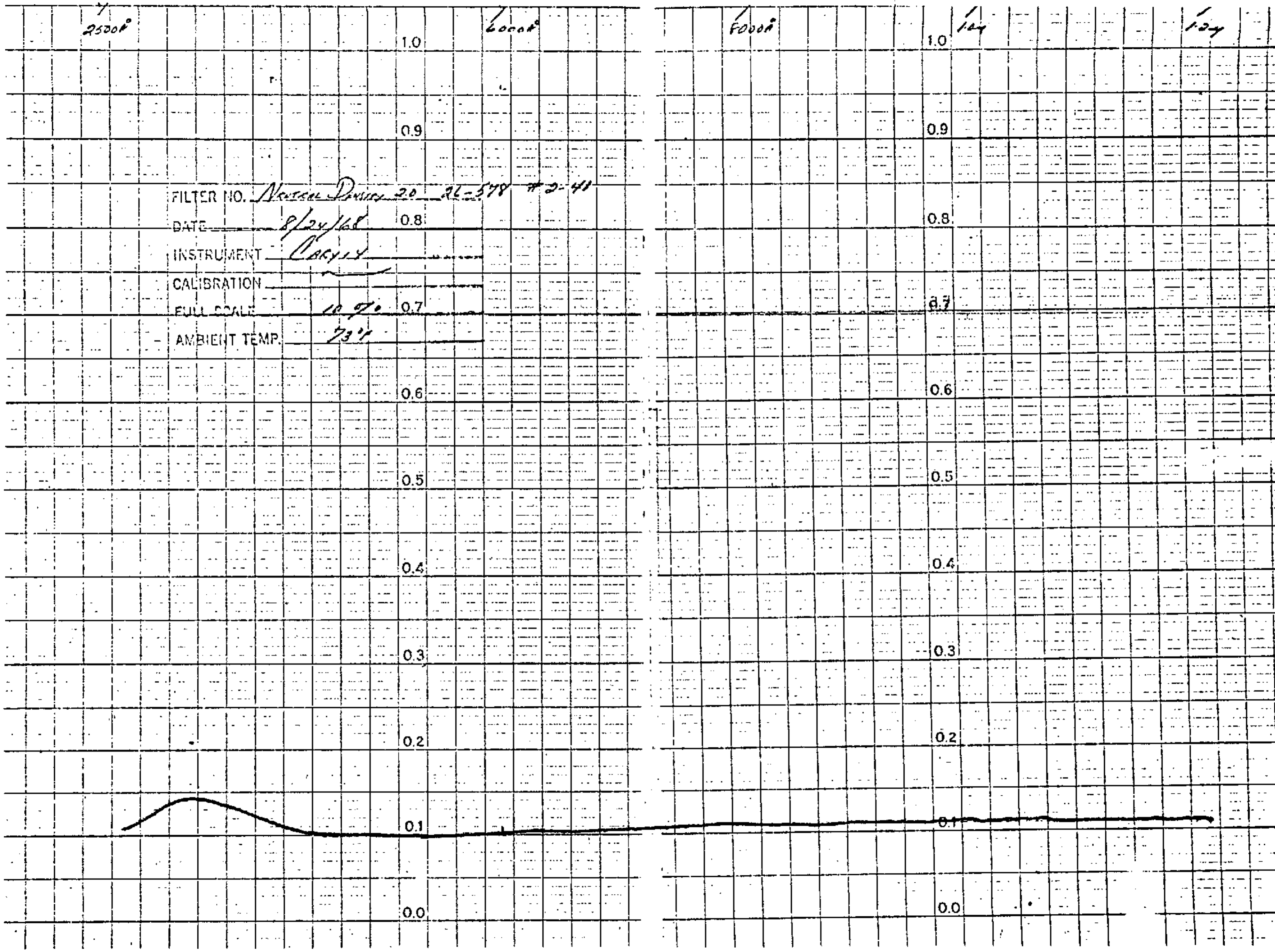


FIGURE 4-8 N.D.2.0 FILTER CURVE

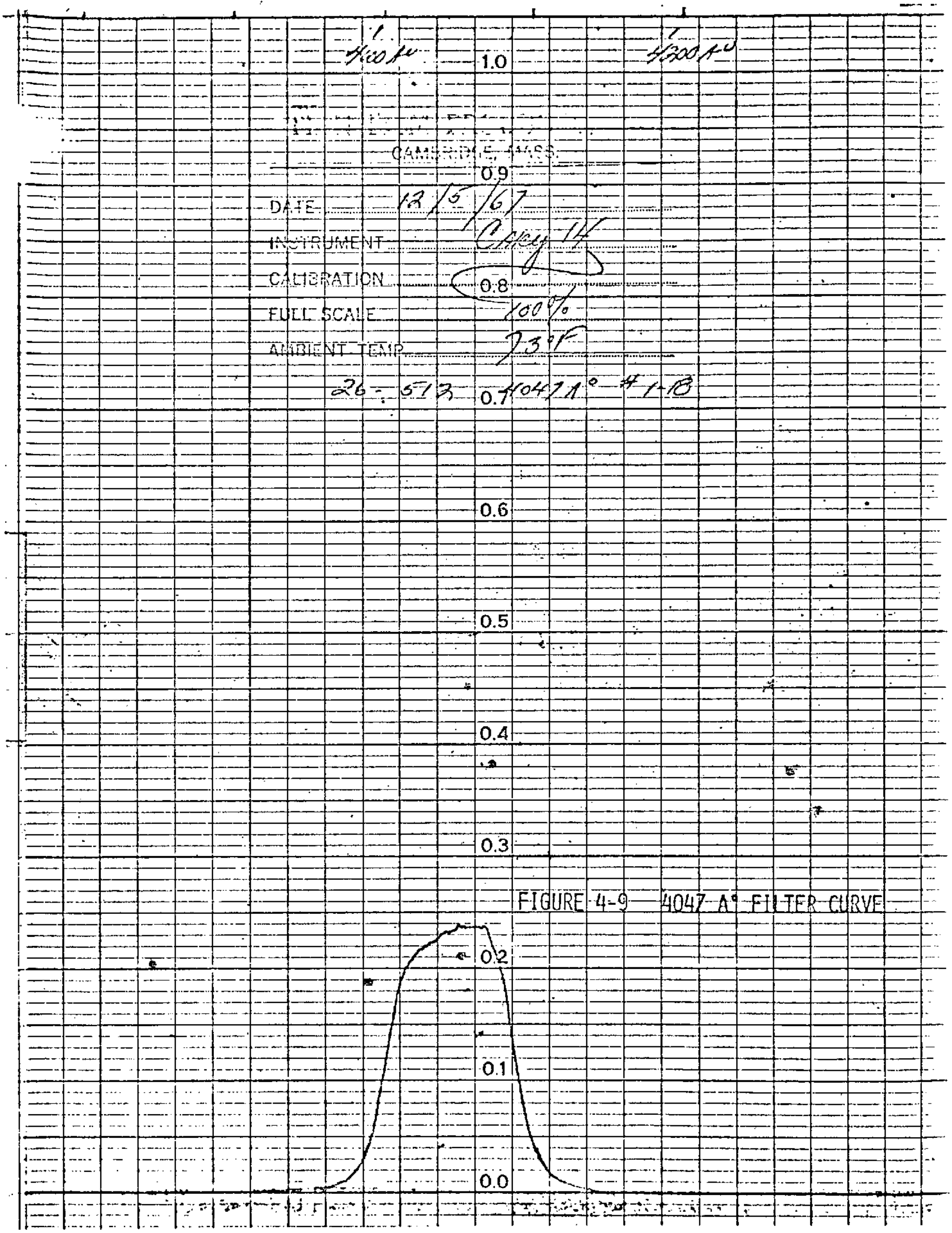


FIGURE 4-9 4047 A° FILTER CURVE

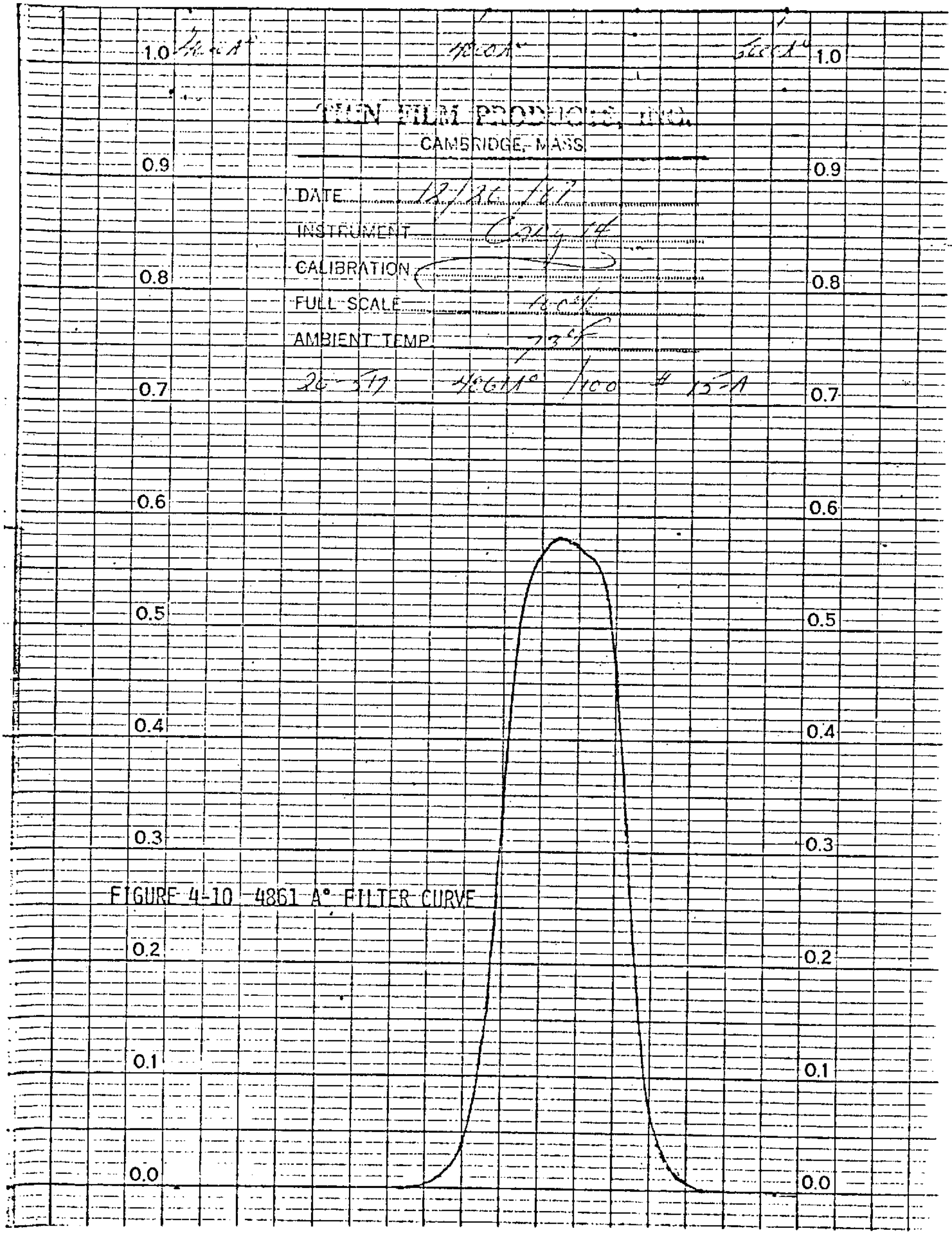


FIGURE 4-10 4861 A° FILTER CURVE

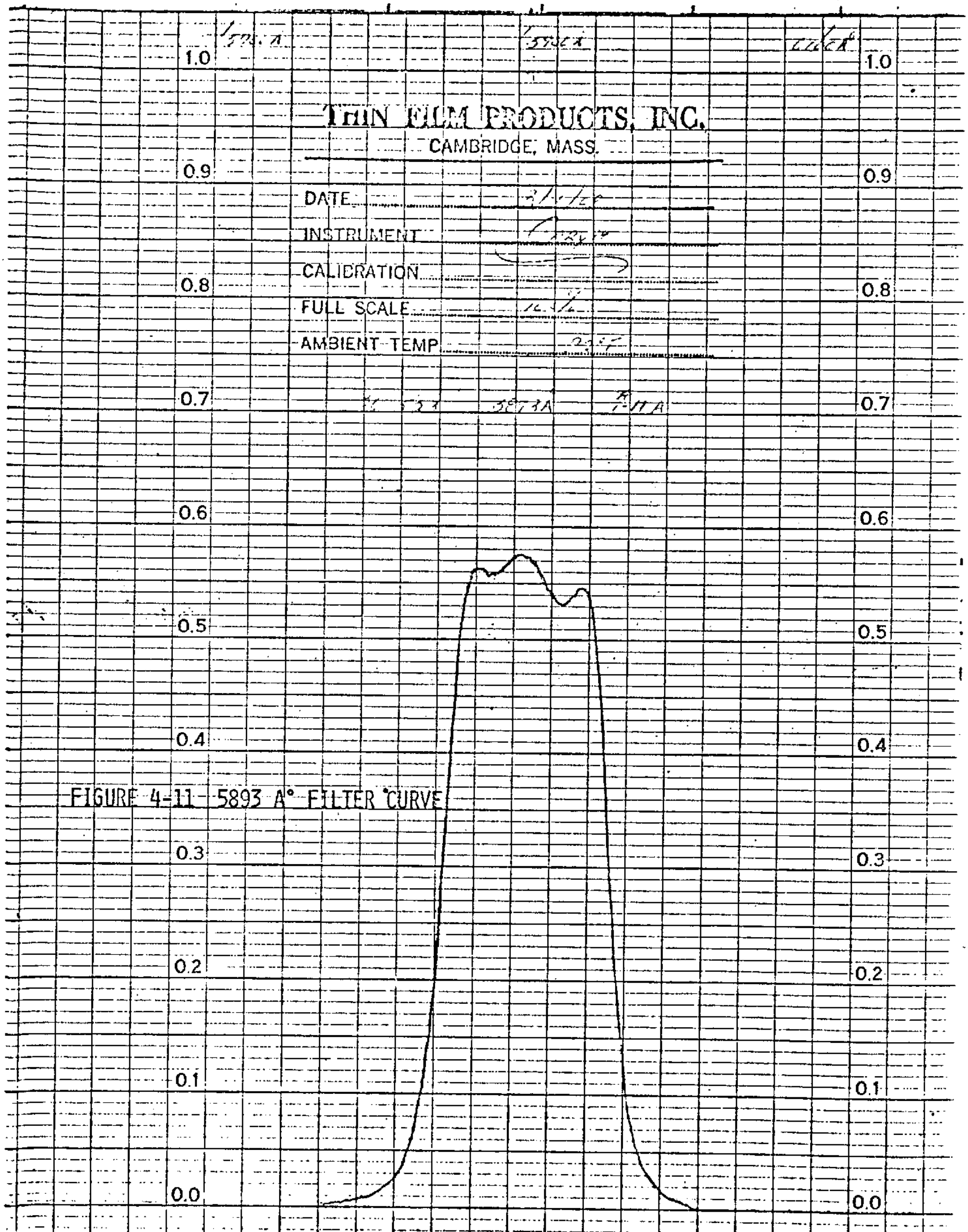


FIGURE 4-11 5893 A° FILTER CURVE

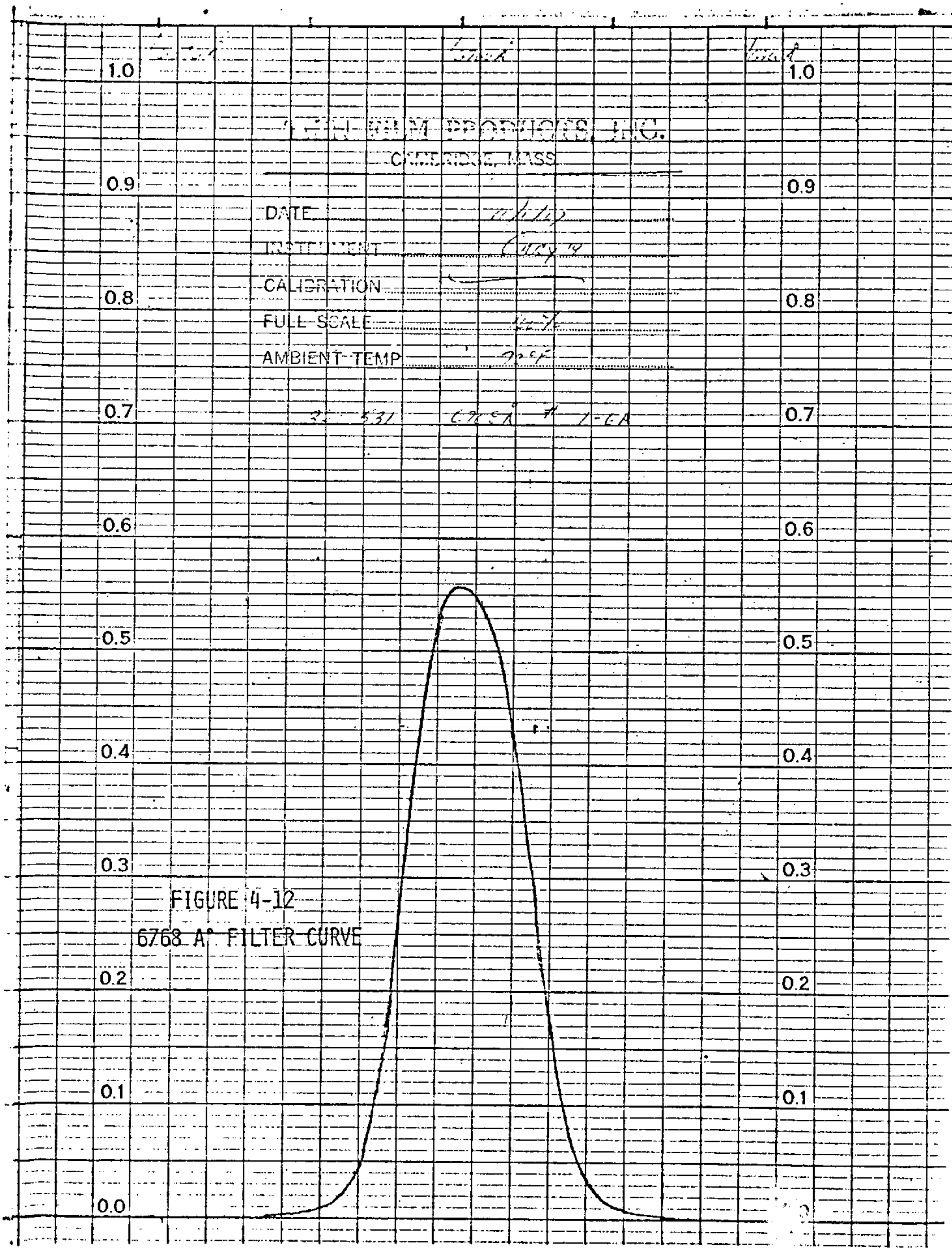


FIGURE 4-12
6768 A° FILTER CURVE

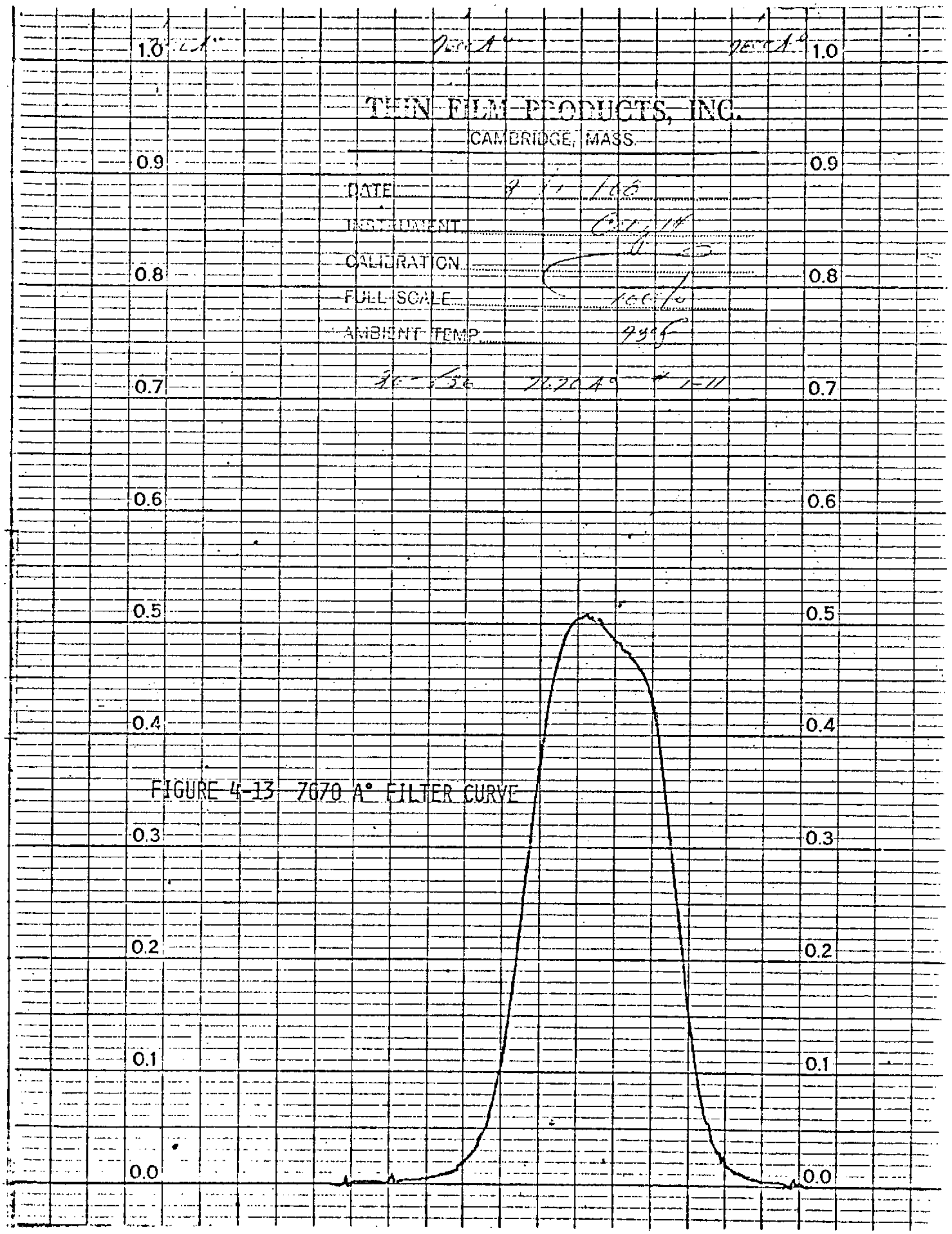


FIGURE 4-13 7670 A° FILTER CURVE

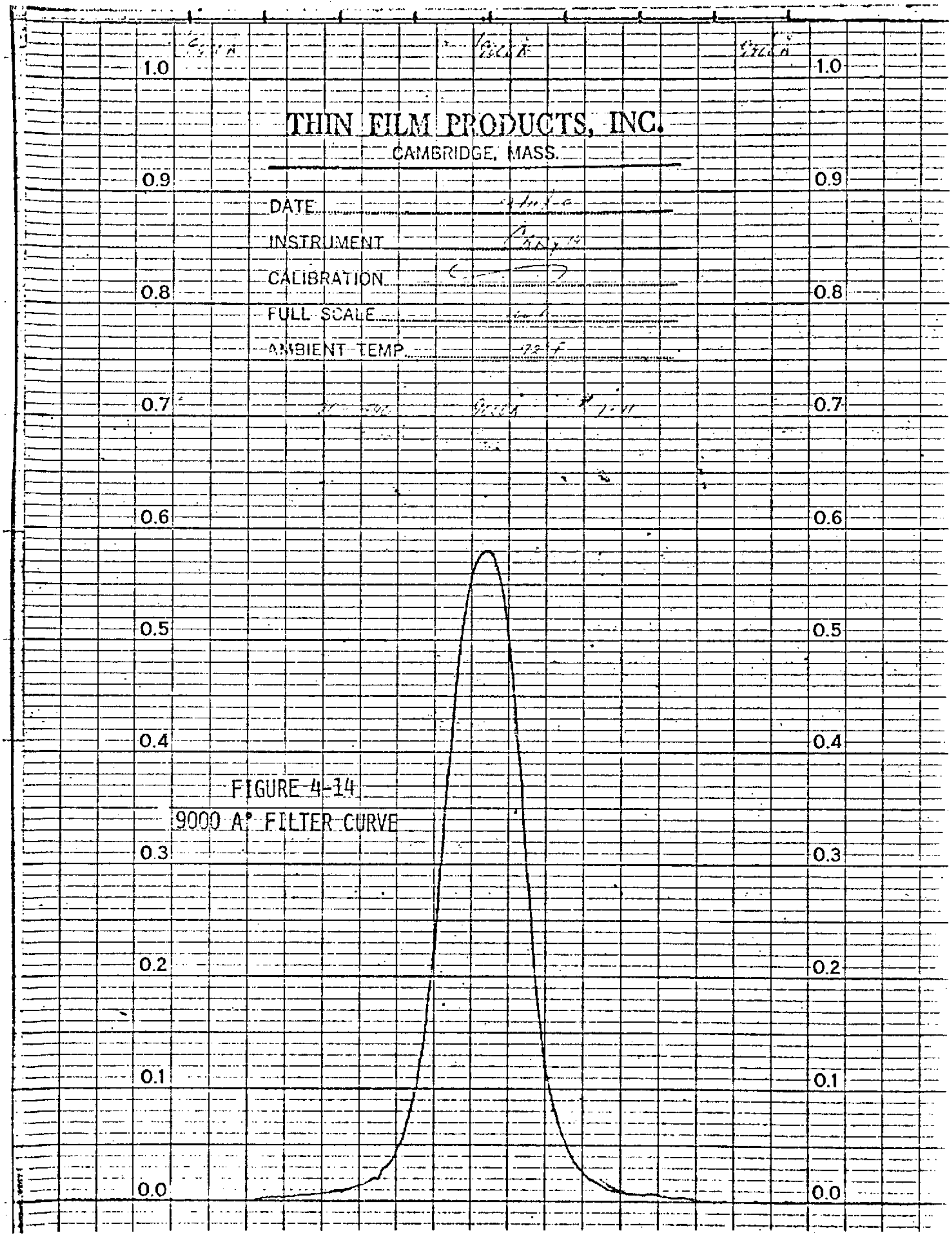


FIGURE 4-14
9000 A° FILTER CURVE

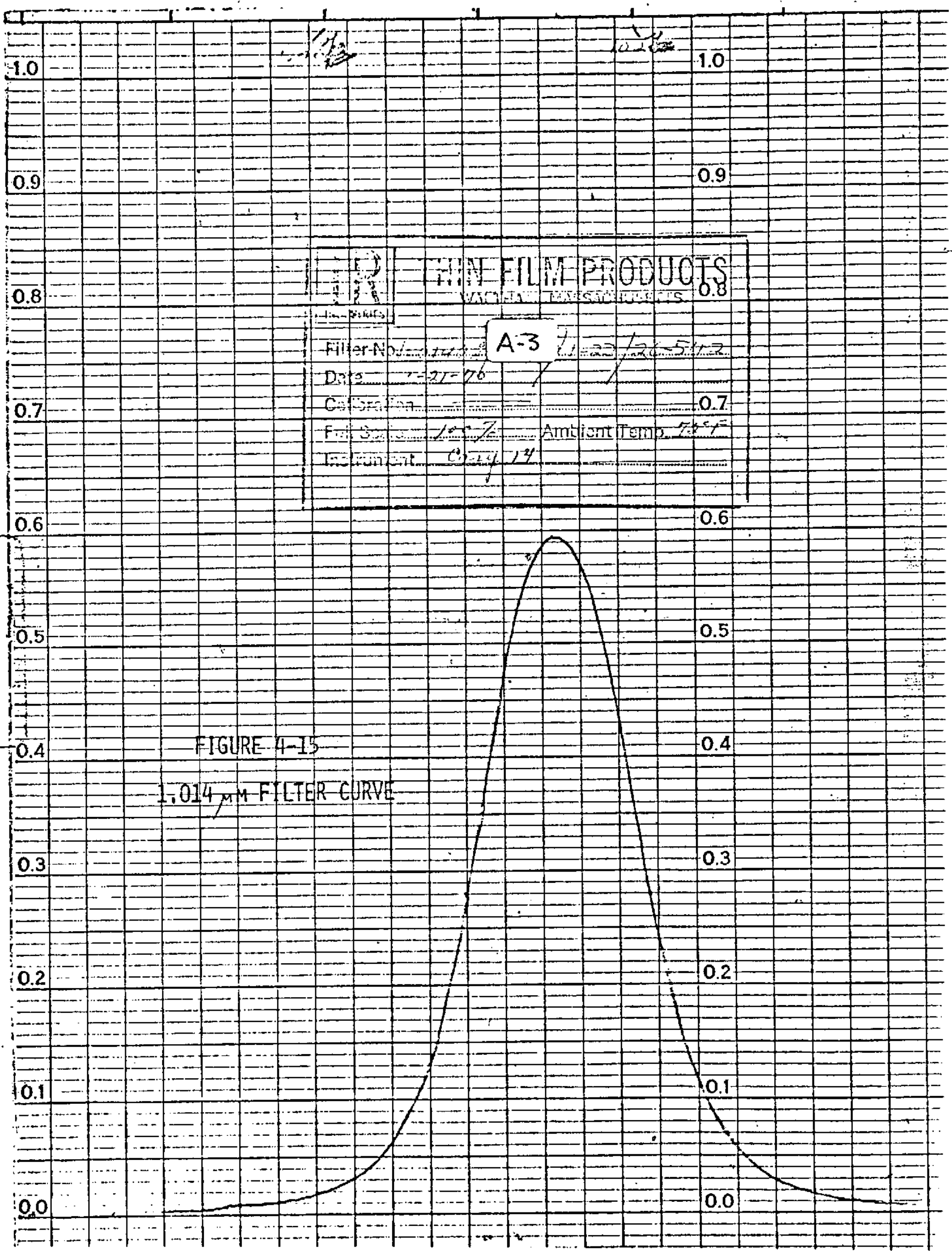


FIGURE 4-15

1.014 μM FILTER CURVE

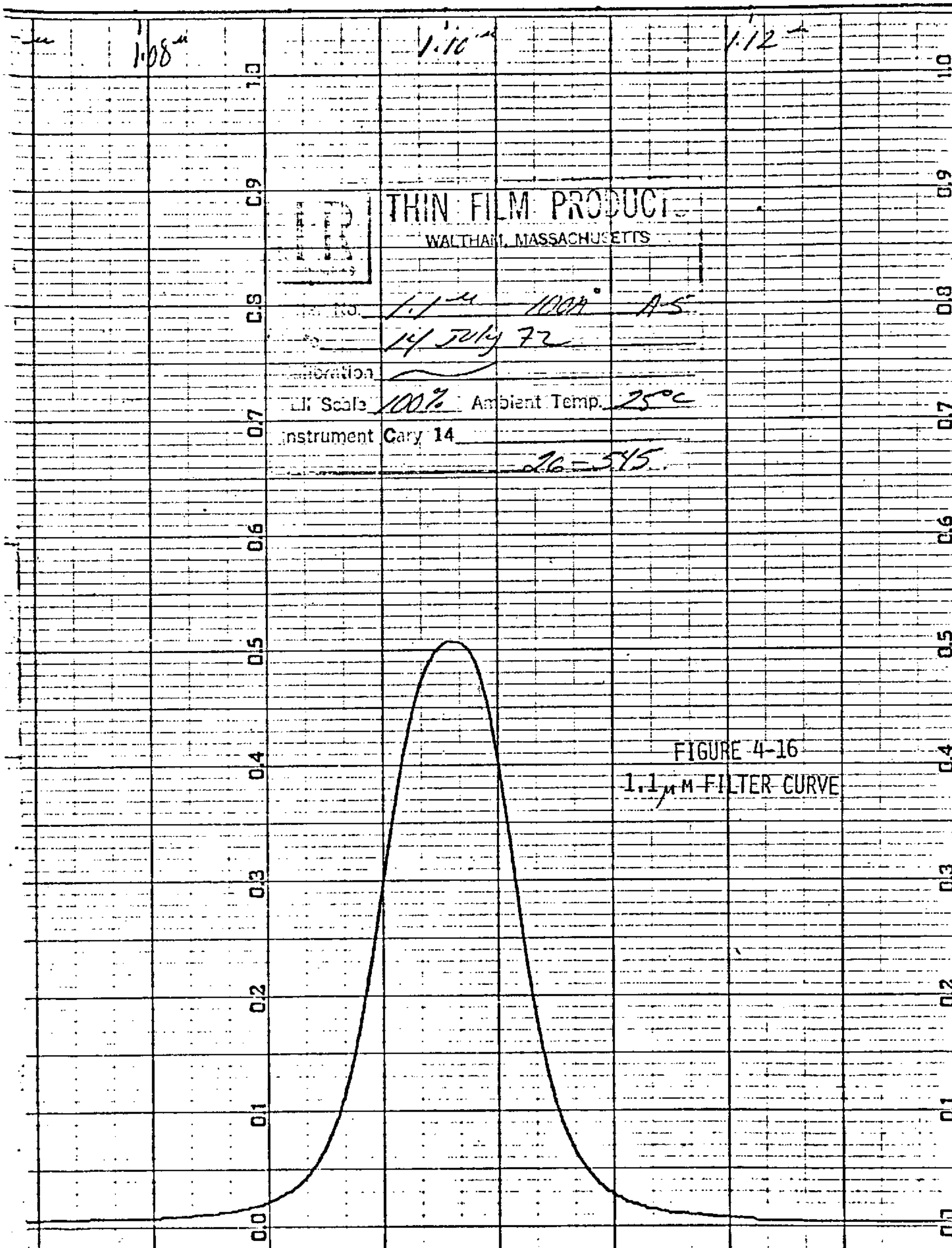


FIGURE 4-16
1.1 μM FILTER CURVE

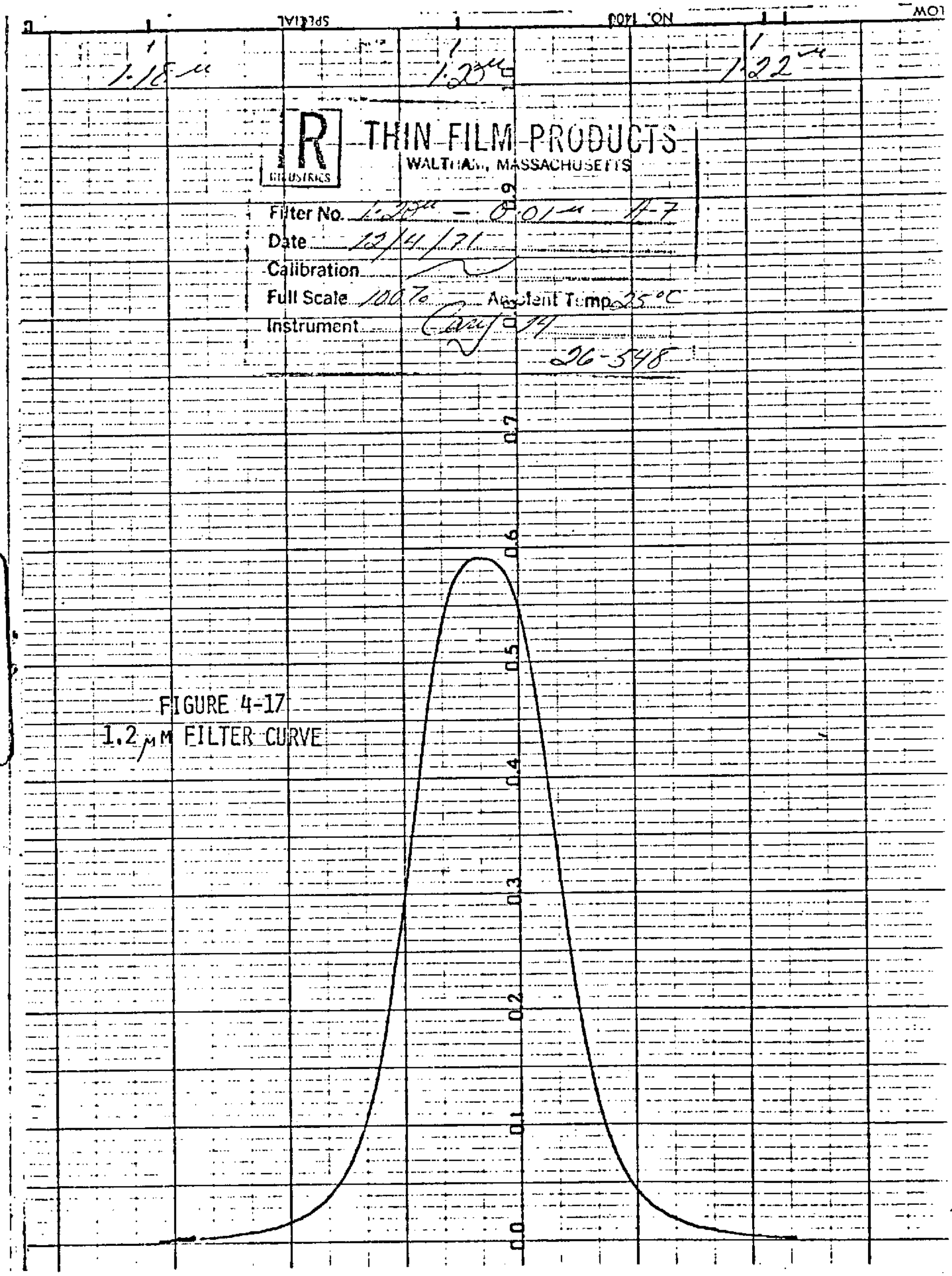


FIGURE 4-17
1.2 µM FILTER CURVE

4.2.4 Array Controller

The array controller is mounted on an optical bench equipment carrier equipped with an X-Y stage for positioning the tested CCLID. The equipment carrier can be moved along the bench.

The controller electronics (CCLID exerciser) can either be operated independently or in conjunction with the automatic test console. It consists of a master oscillator, array clock generating logic, CCLID clock drivers, socket for the CCI under test, and a wide band video amplifier. It is designed to operate at a wide range of clocking frequencies, CCLID voltages, clock waveforms and timing relationship.

4.2.4.1 Oscillator

The oscillator generates the clock train to the CCLID clock generating logic. For a 3 phase CCD, its frequency is set at 3 times the CCLID clocking rate. The oscillator frequency can be manually changed.

4.2.4.2 Logic

The exerciser logic section generates the signals required to operate the CCLID clock drivers and the on-chip amplifier reset driver. The width of the transfer pulses from the CCLID photoelements to its transport register can be varied independent of the clocking frequency. The width and position of the amplifier reset pulse can also be manually adjusted.

The exerciser logic also provides the control signals required for interfacing with the automatic test console.

4.2.4.3 Clock Drivers

The clock drivers accept the logic pulses and convert them into the amplitude and shape required for proper CCI operation. The voltage swing and the fall time of the CCLID clock pulses can be manually adjusted. The swing of the amplifier reset pulse can be adjusted independently. Figure 4-18 shows a schematic diagram of the clock driver circuit.

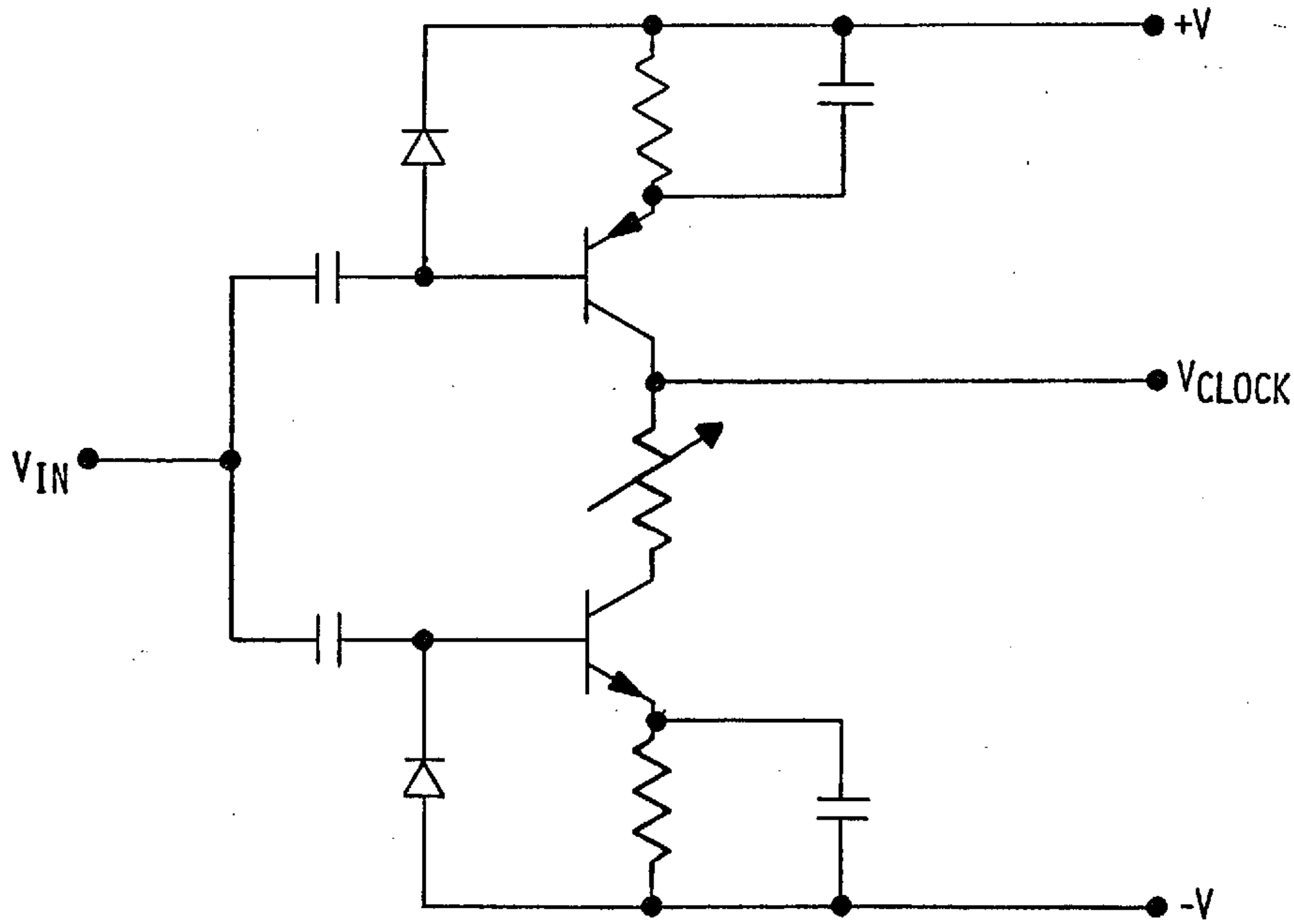


FIGURE 4-18
CLOCK DRIVER CIRCUIT

4.2.4.4 CCLID Socket

A 24 pin DIP socket is mounted on a thermoelectric cooler element, which in turn is mounted on the X-Y stage carrier in the optical bench setup. The socket is pre-wired for all input and output signals of the CCLID. The CCLID under test can be changed merely by unplugging the old unit and inserting the new CCLID in the socket.

4.2.4.5 Video Amplifier

Figure 4-19 is a schematic diagram of the video amplifier used in the CCLID exerciser. This is a wide band amplifier designed to reproduce the CCLID video waveform.

The first stage (A1) is an a.c. coupled inverting amplifier with a gain of 25. The A.C. coupling prevents saturation of the amplifier due to D.C. offsets at the array output, and enables the first stage to amplify the signal only.

The output of A1 is again a.c. coupled to the second stage of the amplifier (A2). The diode CR1 makes use of the fact that the output of each array element is reset to a known level at the on-chip amplifier, and provides a simple clamp to ground for that reference reset level. The second stage A2 has a gain of 0.8, for a total amplifier gain of 20. The potentiometer R is manually set to position the amplifier swing within the range of the A/D converter in the automatic test console. The diode CR2 clips the positive swing of the video reset pulse to prevent saturation of the sample and hold amplifier in the automatic test console.

4.2.5 Automatic Test Console (ATC)

The automatic test console receives the video and sync signals from the array excerciser, converts the video signal into digital form and records the digital data on magnetic tape.

The ATC consists of power supplies, analog to digital converter, memory and control unit and magnetic tape recorder. The computer programs to reduce the recorded data are also an integral part of the ATC.

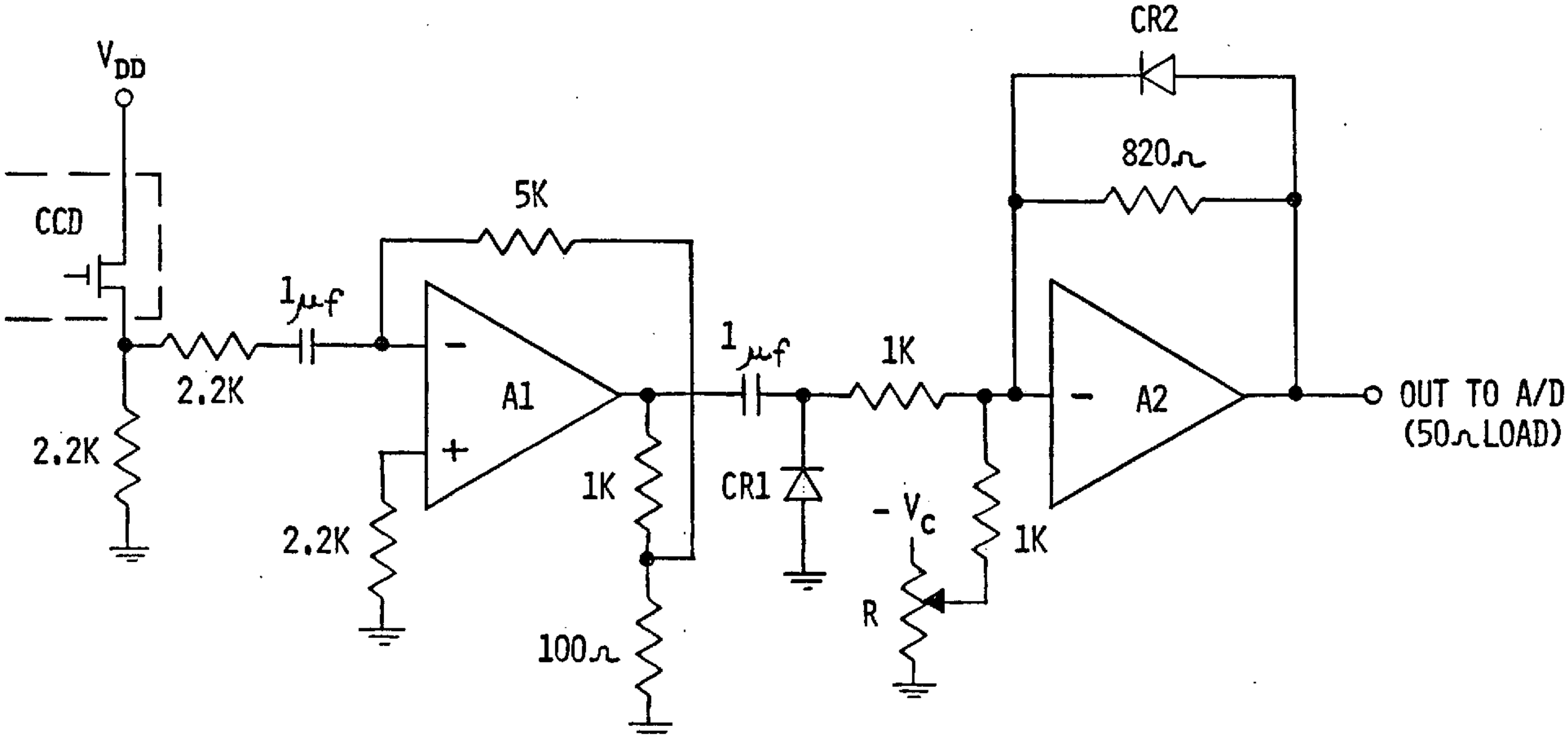


FIGURE 4-19

VIDEO AMPLIFIER

4.2.5.1 Power Supplies

The power supplies in the ATC provide all the DC power required to operate the array excerciser, as well as the power for the ATC's memory, control logic and indicator lights.

4.2.5.2 Analog to Digital Converter

The analog to digital converter system is a Computer Labs model HS-905. It consists of a sample and hold amplifier followed by a 9 bit A/D converter. This unit operates asynchronously at a conversion rate of up to 5 MHz with an accuracy of 0.1% ± 1/2 least significant bit. Its analog input voltage range is 0 to -2.048 volts, for a least significant bit weight of 4.0 mV. The system is triggered by a 50 ns long "convert command" signal, generated by the ATC control logic. The conversion time is 180 ns. The A/D converter's dynamic range is 512:1.

4.2.5.3 Memory and Control Unit

The memory and control unit coordinates the functions of the ATC. It continuously maintains synchronism with the array controller by means of clock counts to corrolate each portion of the video stream with the CCLID element producing it. The "convert command" to the A/D converter is generated by the control unit and can be manually adjusted to sample the desired portion of the element video output.

The unit's control panel contains a series of digital thumbwheel switches. These are set by the operator to identify the type of test, light level identification and the number of data points taken per test condition for each detector position. (manually variable from 1 to 99).

When a test cycle is initiated, the control unit generates a "convert command" pulse to the A/D converter for each of the CCLID element's output. At the end of each conversion, the 9 bit output of the A/D converter is transferred into a buffer memory. After all the array elements are converted and stored, the control unit forwards the content of the buffer memory, along with the test conditions set on the thumbwheel switches, to the magnetic tape recorder. This sequence is then repeated until the number of samples of each element coincide with the number preset on the control panel.

When the test cycle is completed, test conditions are changed, identified on the thumbwheel switches and a new test cycle is initiated.

4.2.5.4 Magnetic Tape Recorder

The magnetic tape recorder is a Hewlett-Packard Model 7970 digital magnetic tape unit. It contains both read and write electronics and performs a read-after-write validity check on the recorded data.

The recorder produces a computer compatible magnetic tape using NRZ format at 800 bytes per inch.

4.2.5.5 Computer Programs

A set of computer programs was developed, to process the tapes containing the test data and generate a computer printout of the reduced data.

The programs include generation of mean signal for the signal transfer curve, uniformity information, and computed RMS noise. The tapes are processed on an IBM 360/50 computer.

4.2.6 Manual Monitoring Equipment

The manual monitoring equipment is used for monitoring and adjusting operating parameters and for manual tests. The monitoring instruments include: a) digital voltmeter, b) Tektronix Model 545 oscilloscope with one type W differential plug-in for measurements at low signal levels and one dual trace plug-in, c)Polaroid Camera

4.2.7 Light Probe

The light probe is used to generate a small light spot and image it on a selected array element. It consists of a trinocular microscope which allows viewing through a standard binocular pair and projection of a light spot through the third leg. A beam splitter in the microscope enables simultaneous projection and viewing. A photograph of the light probe is shown in figure 4-3.

The light source is a Sylvania C2T tungsten arc lamp, about .010" in diameter. The source is reduced through an eyepiece and a microscope objective to about 5-10 μm in diameter, and imaged on the array surface. An X-Y stage at the base of the microscope provides the means of positioning the light spot on any desired element of the array.

The light probe is used for the element profile test, crosstalk test and the charge transfer efficiency test. For the transfer efficiency test, a filter (0.5 to 0.6 μm) is placed under the light source. This restricts the irradiance to short wave lengths, and minimizes the effects of electrical crosstalk between detector positions on transfer efficiency measurements. The light intensity is varied by insertion neuteral density filters in the light path.

4.3 THERMOELECTRIC DEVICE

During temperature tests the array temperature was maintained through the use of a Cambion Model 806-1000-01 thermoelectric device, in conjunction with a Cambion Model 809-1000-01 bipolar controller. The controller maintains the device temperature stability to ±0.1°C at an ambient temperature of 10°C to 35°C and an array temperature of 0°C to 50°C. The CCLID temperature was monitored by a Lewis Engineering Company Model 14P0 pyrometer, with an accuracy of ±1°F.

The CCLID socket is mounted on a solid copper block, which in turn is attached to the active surface of the thermoelectric device. The copper block protrudes through an opening in the socket, to make thermal contact with the back of the CCLID ceramic package. All thermal contact surfaces are coated with silicone grease to maintain uniform thermal contact.

Figure 4-20 shows the thermoelectric device assembly, mounted on the light probe's X-Y stage, with a CCLID inserted in the socket.

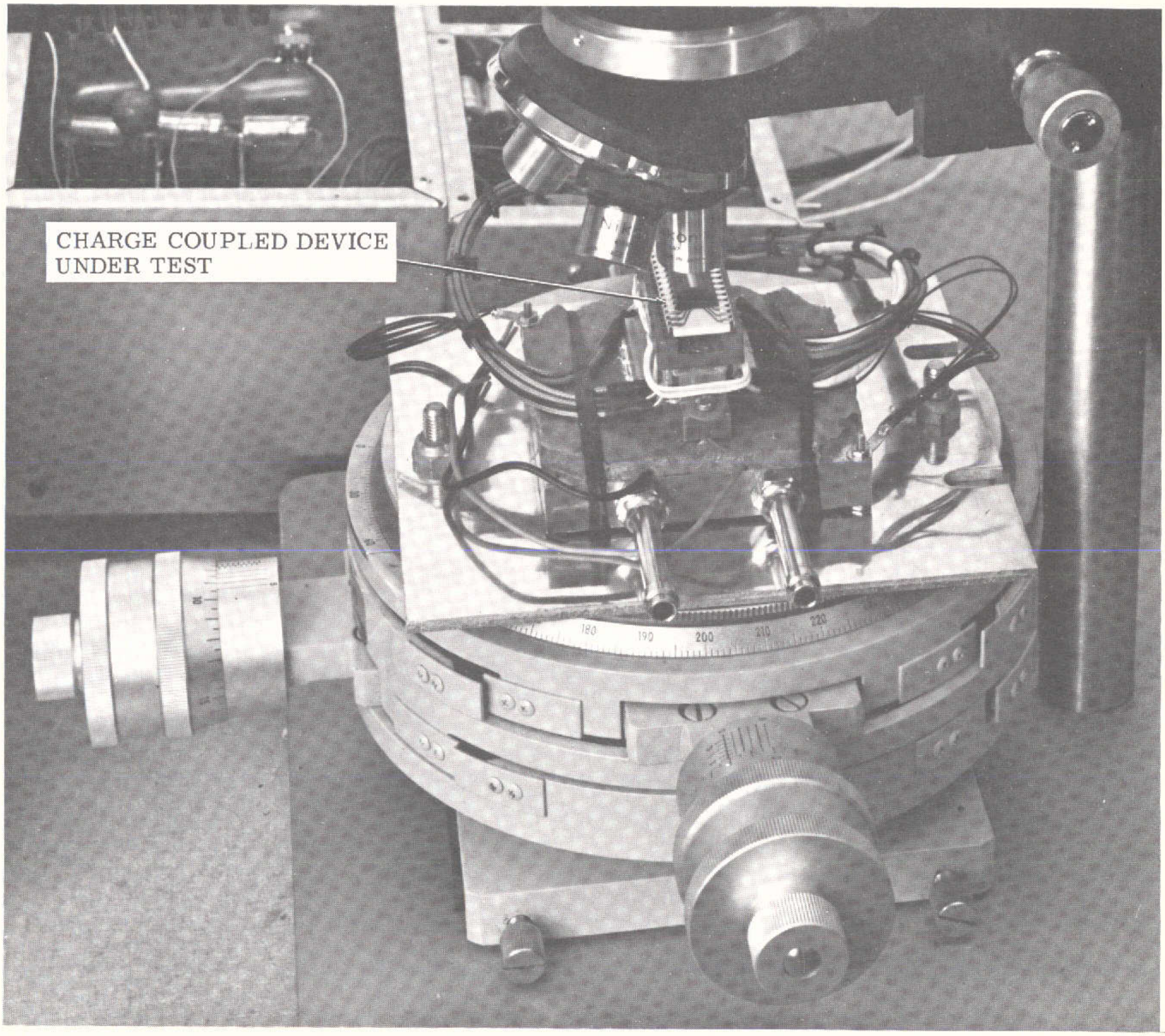


FIGURE 4-20. THERMOELECTRIC DEVICE

SECTION 5

TEST PROCEDURES

5.1 GENERAL

This section describes the procedures used in the various tests performed on the CCLID's and the methods used in calibrating the test setup. The test results and their analysis are described in Section 6.

5.2 TEST SETUP CALIBRATION

The test setup and its component were calibrated prior to the start of the tests. Standard electronic test equipment such as digital voltmeters and oscilloscopes underwent a routine calibration procedure by Fairchild's quality control department. Specialized equipment, such as the A/D Converter system and the spectroradiometer were sent to the manufacturers for calibration. The optical setups which were made explicitly for the CCLID tests were calibrated at the CCD test labs by project personnel. The following paragraphs describe the calibration procedures for these equipments.

5.2.1 Diffused Light Source

The radiant flux density produced by the diffuse light source and incident on the surface of the CCLID was measured with a spectroradiometer in the spectral band of .4 to 1.2 μm, corresponding to the spectral bandwidth of silicon. The spectroradiometer provides the spectral flux density in watts/cm^{2}nm at the measured wavelength. Measurements were taken at 20 nm intervals. The resulting curve (see Figure 4-4) shows the amplitude of the flux density at the given wavelengths. The area under the curve equals the total radiant flux density in watts/cm^2 for the silicon spectral bandwidth.

The measurements were taken with the spectroradiometer at a distance of 142.75 cm from the diffuse aperture. The total irradiance at this point was 6.5913 uW/cm^2 (2854°K source). Using the inverse square law, the light can be calculated for any other position on the optical bench. The inverse square law, however, does not hold true when the distance from the source is less than 10 times the source diameter. The aperture used has a diameter of 19 mm. The minimum distance between the array and the source, therefore, cannot be less than 19 cm. During tests, the minimum distance used was about 42 cm.

The limited length of the optical bench (2 meters) permits a light variation of 25:1. The neutral density filters were used to further attenuate the light source intensity. The filter transmission curves (Figures 4-7 and 4-8), varies slightly with wavelength. To find the exact attenuation factor on silicon, a CCLID was used to calibrate the filters.

5.2.1.1 N.D. 1.0 Filter Calibration

The procedure used to calibrate the N.D. 1.0 filter was as follows:

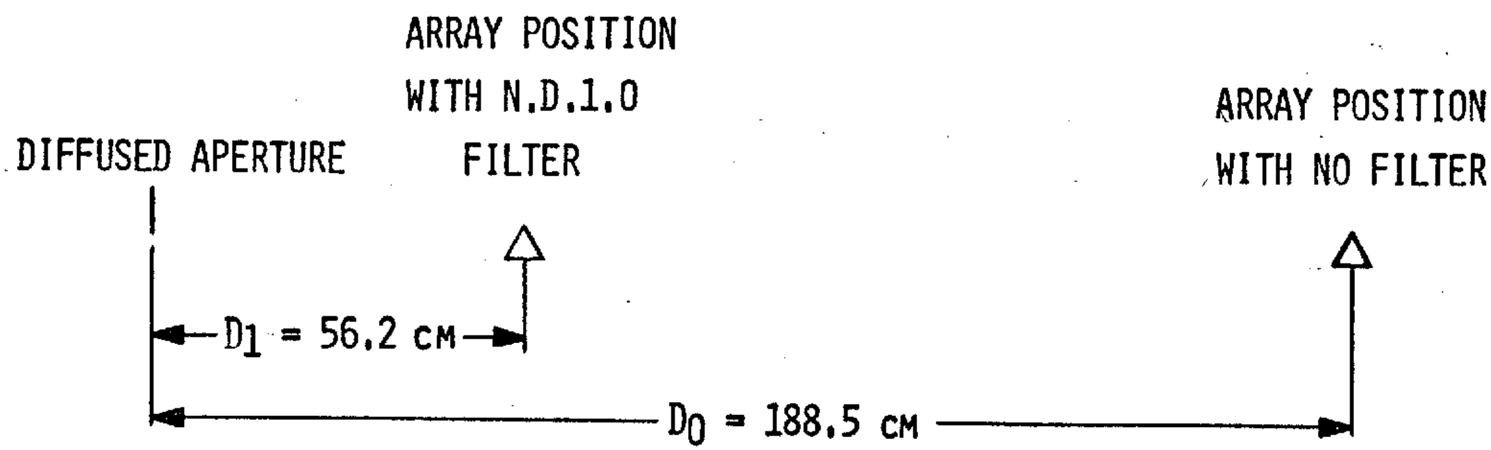
(a) The CCLID was placed at a known distance from the diffused light source. The bench position (D_0) and the response of a selected array element were recorded.

(b) The N.D. 1.0 filter was placed in the light path. The CCLID was moved towards the light source until the selected element response was the same as in (a). The new bench position (D_1) was recorded.

(c) Since the irradiance at the CCLID in positions (a) and (b) is equal, the filter transmission factor ($T_{1.0}$) can be calculated using the inverse square law

$$T_{1.0} = \left(\frac{D_1}{D_0}\right)^2$$

Figure 5-1 shows a diagram of the bench positions during the calibration of the N.D. 1.0 filter and the resulting transmission factor for this filter.



$$T_{1.0} = \left(\frac{D_1}{D_0}\right)^2 = \left(\frac{56.2}{188.5}\right)^2 = 0.0889$$

FIGURE 5-1 N.D.1.0 FILTER CALIBRATION

5.2.1.2 N.D. 2.0 Filter Calibration

The N.D. 2.0 filter was calibrated using a similar procedure.

(a) The CCLID was placed at a known distance from the diffused light source. The precalibrated N.D. 1.0 filter was inserted in the light path. The bench position (D_0) and the response of a selected array element were recorded.

(b) The N.D. 2.0 filter was placed in the light path instead of the N.D. 1.0 filter. The CCLID was moved towards the light source until the selected element response was the same as in (a). The new bench position (D_1) was recorded.

(c) Since the irradiance at the CCLID in position (a) and (b) is equal, the ratio of the transmission factors of the two filters is proportional to the square of the ratio of the array distances.

$$\frac{T_{2.0}}{T_{1.0}} = \left(\frac{D_1}{D_0}\right)^2$$

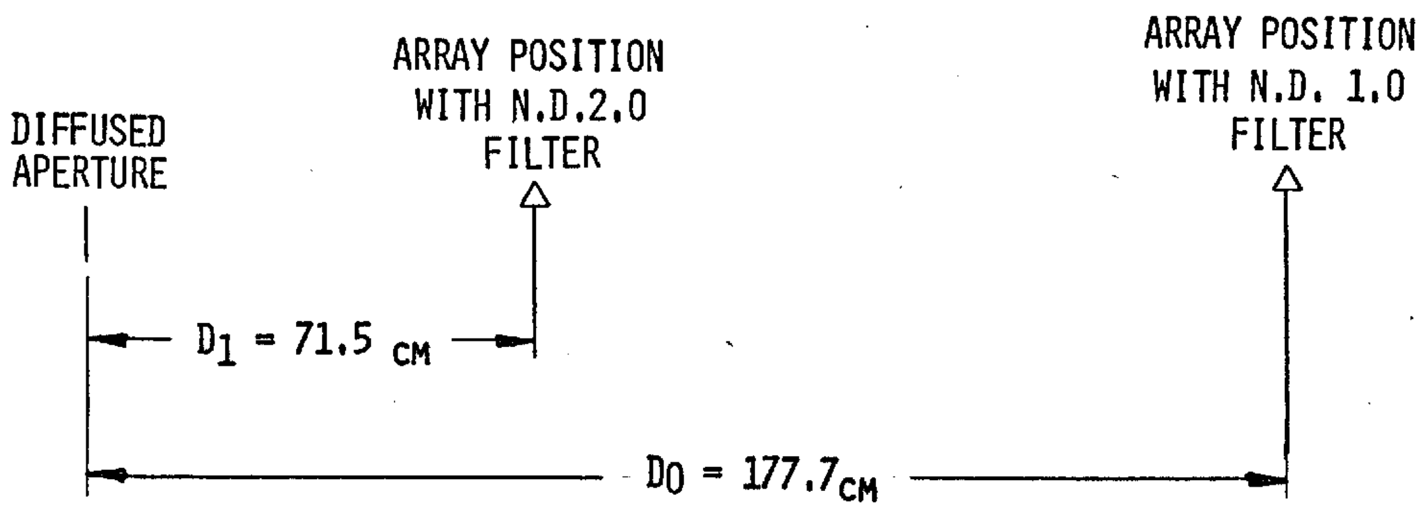
or

$$T_{2.0} = T_{1.0}\left(\frac{D_1}{D_0}\right)^2$$

Figure 5-2 shows a diagram of the bench positions during the calibration of the N.D. 2.0 filter and the resulting transmission factor for that filter.

5.2.1.3 Selection of Test Irradiance Levels

A set of 17 bench position-filter combination was selected and the irradiance at the array surface was calculated for each. The calculated points covered a light dynamic range of 1000:1. The irradiance at the center of the range was arbitrarily called unity irradiance. For this light level, the array was placed at a distance of 59.6 cm from the diffused light source, and no filter was used.



$$T_{2.0} = T_{1.0}\left(\frac{D_1}{D_0}\right)^2 = 0.0889\left(\frac{71.5}{177.7}\right)^2 = 0.0144$$

FIGURE 5-2 N.D.2.0 FILTER CALIBRATION

From the spectro-radiometer measurements it is known that at a distance

$$D_s = 142.75\text{cm}$$

the irradiance at the array is

$$I_s = 6.5913 \text{ uW/cm}^2 = 6.5913 \times 10^{-2} \text{ w/m}^2 \text{ (2854°K source)}$$

The arbitrary unity irradiance was selected to be at a distance

$$D_1 = 59.6 \text{ cm}$$

from the light source (see Figure 5-3).

Using the inverse square law, the unity irradiance (I_1) at this distance is

$$\frac{I_1}{I_s} = \left(\frac{D_s}{D_1}\right)^2$$

therefore,

$$I_1 = I_s\left(\frac{D_s}{D_1}\right)^2 = 6.5913 \times 10^{-2}\left(\frac{142.75}{59.6}\right)^2 = 37.8 \times 10^{-2} \text{ w/m}^2$$

For an integration time of

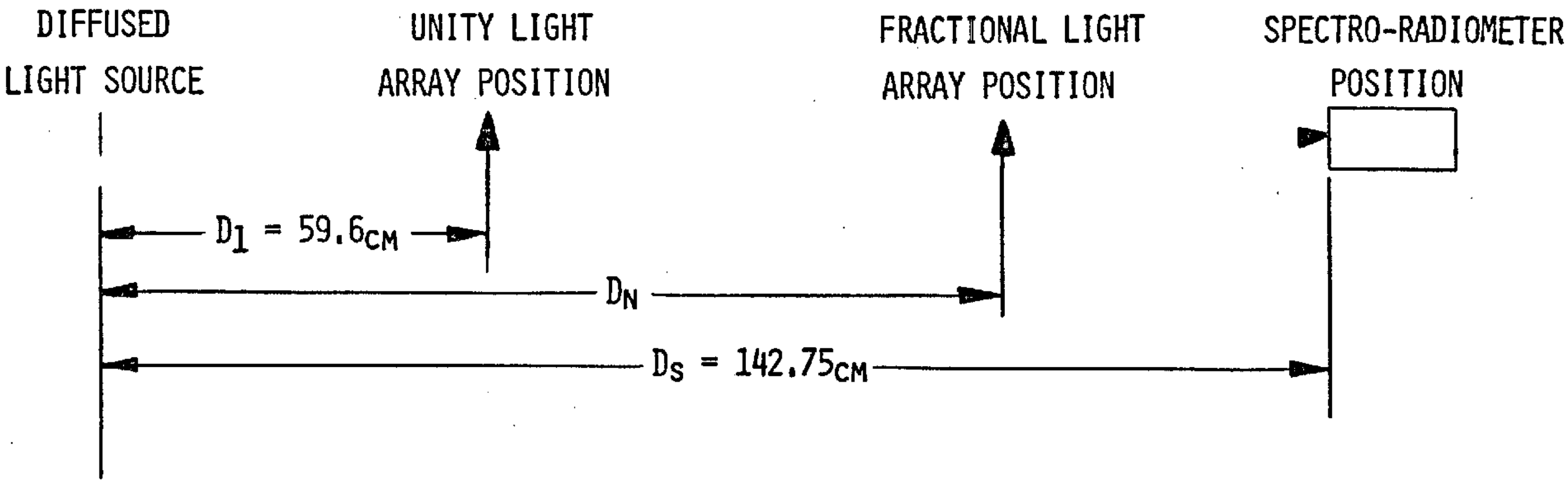
$$T_i = 2 \text{ msec}$$

The unity energy (E_1) at the array is

$$E_1 = I_1 T_i = 37.8 \times 10^{-2} \cdot 2 \times 10^{-3} = 756 \times 10^{-6} \text{ J/m}^2$$

To calculate the bench positions (D_n) for the remaining selected test irradiance levels, the inverse square law is again used. For this calculation,

$$\frac{E_n}{E_1} = \text{Fraction of Desired Energy}$$



$$E_1 = E_S \left(\frac{D_S}{D_1}\right)^2$$

$$D_N = D_1 \sqrt{\frac{E_1}{E_N}\, T_N}$$

FIGURE 5-3 CALCULATION OF SELECTED IRRADIANCE LEVELS and

$$T_n = \text{Filter Transmission Factor}$$

When no filter is used

$$T_n = 1.0$$

When N.D. 1.0 filter is used

$$T_n = T_{1.0} = 0.0889$$

When N.D. 2.0 filter is used

$$T_n = T_{2.0} = 0.0144$$

The desired distance is:

$$D_n = D_1 \sqrt{\frac{E_1 T_n}{E_n}} = 59.6 \sqrt{\frac{E_1}{E_n} \cdot T_n}$$

Figure 5-3 shows a diagram of the bench positions used for this calculation. Table 5-1 lists the selected irradiance levels in absolute values and as a ratio of the unity irradiance, the filter used with each level, the filter transmission factor and the array distance from the diffused light source. In that table, the bench position for 1/10 of unity irradiance is calculated for two conditions - when no filter is used, and when a N.D. 1.0 filter is used. Similarly, the bench position for 1/100 of unity irradiance is derived with a N.D. 1.0 and with a N.D. 2.0 filter.

5.2.2 Narrow Band Irradiance

The intensity of the monochromatic light used for the spectral response test was calculated from the spectroradiometer measurements of the undiffused light source (Figure 4-5), the filter transmission curves (Figures 4-9 through 4-17), and the distance between the array and the light source.

The undiffused light was measured with the spectroradiometer at a distance of

$$D_s = 173.9 \text{ cm}$$

TABLE 5-1

CONDITIONS FOR SELECTED IRRADIANCE LEVELS

Irradiance Level (E_n-uJ/M^2) (2854°K)	Irradiance Ratio (E_n/E_1)	Filter Type	Filter Transmission Factor (T_n)	Distance (D_n - cm)
1512	2	None	1.0	42.2
1134	1.5	None	1.0	48.7
832	1.1	None	1.0	56.8
756	1.0	None	1.0	59.6
504	1/1.5	None	1.0	73.0
378	1/2	None	1.0	84.3
151	1/5	None	1.0	133.3
76	1/10	None	1.0	188.5
76	1/10	N.D. 1.0	0.0889	56.2
30	1/25	N.D. 1.0	0.0889	88.8
15	1/50	N.D. 1.0	0.0889	125.6
7.6	1/100	N.D. 1.0	0.0889	177.7
7.6	1/100	N.D. 2.0	0.0144	71.5
5.0	1/150	N.D. 2.0	0.0144	87.6
3.8	1/200	N.D. 2.0	0.0144	101.1
2.5	1/300	N.D. 2.0	0.0144	123.8
1.5	1/500	N.D. 2.0	0.0144	159.8

The spectral response measurements were taken with the array in two different positions (see Figure 5-4). For wavelengths at the ends of the silicon response bandwidth, the distance used was

$$D_1 = 58.35 \text{ cm}$$

For wavelengths at the center of the silicon band the distance used was

$$D_2 = 106.15 \text{ cm}$$

To correct the intensity for the different distances, two correction factors K_1 and K_2 were derived for the group 1 and group 2 filters respectively.

For group 1,

$$K_1 = \frac{I_1}{I_s} = \left(\frac{D_s}{D_1}\right)^2 = \left(\frac{173.9}{58.35}\right)^2 = 8.88$$

and for group 2,

$$K_2 = \frac{I_2}{I_s} = \left(\frac{D_s}{D_2}\right)^2 = \left(\frac{173.9}{106.15}\right)^2 = 2.68$$

The intensity of each irradiance wavelength at the test distance is

$$I_{\lambda i} = K_i \, I_{\lambda s} \quad \text{Watts/cm}^2 \cdot \text{nm}$$

Where $I_{\lambda s}$ for the test wavelengths is obtained from the lamp emission curve, Figure 4-5.

The total transmission factor (T_λ) of the narrow band filters is defined as the area under the filter transmission curve (Figures 4-9 through 4-17). The light amplitude at the test wavelength ($I_{\lambda i}$) is given in Watts/cm^2-nm. The product of the two provides the total narrow band irradiance at the array in Watts/cm^2

$$I_{fi} = T_\lambda \, I_{\lambda i} = K_i \, T_\lambda \, I_{\lambda s}$$

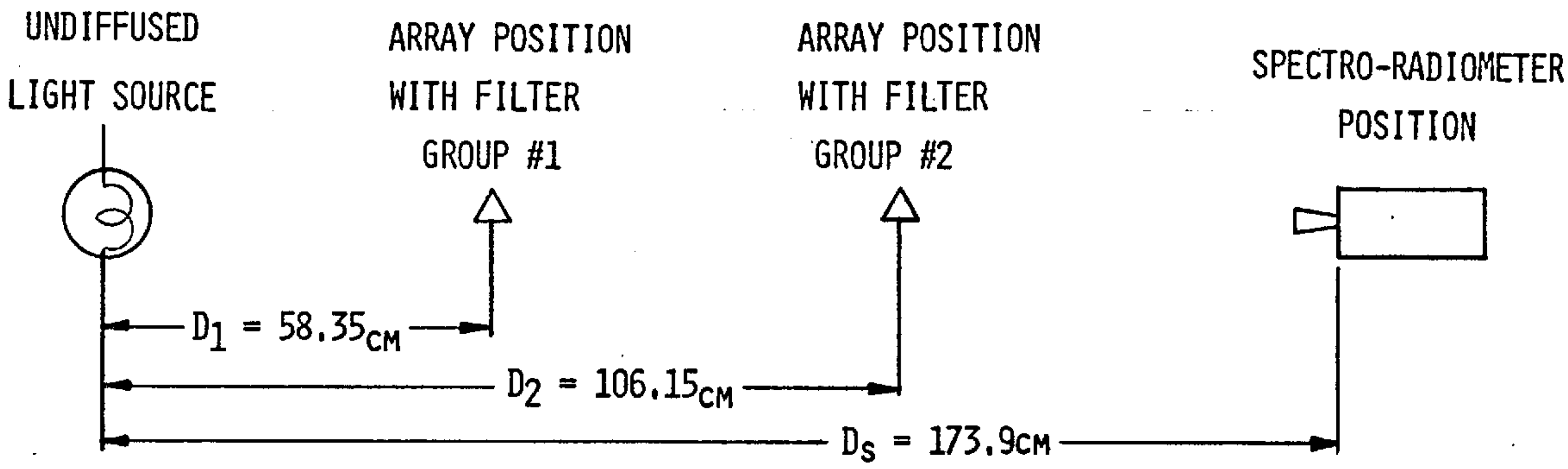


FIGURE 5-4 BENCH POSITIONS FOR SPECTRAL RESPONSE TEST.

Table 5-2 lists the filters center wavelengths (λ_c), their transmission factor (T_λ), the filter group, the distance correction factor (K_i), the intensity measured with the spectroradiometer at the center wavelength ($I\lambda_s$) and the total narrow band irradiance at the array (I_{fi}).

5.3 TEST PROCEDURES

The following paragraphs describe the procedures used in the various CCLID tests.

5.3.1 Charge Transfer Efficiency

The charge transfer efficiency is defined as the percentage charge remaining in a CCD storage element after one transfer.

Charge was introduced into a single photosensitive element by illuminating that element with a small light spot, approximately 5 µm in diameter. The light spot was produced by the specially designed light probe described in paragraph 4.2.7.

The signal amplitude of the illuminated element was measured at the output of the CCLID. The signal amplitude of the elements trailing the illuminated element was also measured. These outputs contain the charge loss of the illuminated element due to transfers through the transport registers to the array output.

To measure the transfer efficiency over a known number of transfers, the light spot was placed on one photoelement at the beginning of the CCLID and one photo-elementat the end. The main and trailing signals of each illuminated element were measured and provide the basic data for calculating the transfer efficiency.

The transfer efficiency was measured for CCLID 60 and CCLID 500 odd and even transport registers.

For CCLID 500, the measurement was performed with a clocking rate of 250KHz, and at a light level of 0.5 and 0.25 of saturation. For the odd transport register, the light spot illuminated elements 1 and 499. For

TABLE 5-2

NARROW BAND LIGHT INTENSITIES

Center Wavelength λ_c (nm)	Filter Factor T_λ (nm)	Filter Group i	Distance Correction Factor K_i	Measured Irradiance $I_{\lambda s}$ (uW/cm^2 nm)	Test Irradiance I_{fi} (uW/cm^2) (2854°K)
404.7	2.8	1	8.88	0.135	3.36
486.1	5.12	1	8.88	0.390	17.72
589.3	5.46	2	2.68	0.820	11.96
670.8	5.08	2	2.68	1.180	16.05
767.0	5.27	2	2.68	1.490	21.00
900.0	7.58	2	2.68	1.650	33.51
1014.0	7.54	1	8.88	1.420	95.00
1100.0	5.48	1	8.88	1.170	56.90
1200.0	6.63	1	8.88	1.120	65.90

the even transport register, the light spot illuminated elements 2 and 500. The main and two trailing signals for these elements were recorded.

For CCLID 60, the clocking frequency was increased to 500KHz, since the array is too short to show a measurable inefficiency at low clocking rates. The light level was set at 0.5 of saturation. For the odd transport register, the light spot illuminated elements 3 and 57. For the even register, the light spot illuminated elements 4 and 58. The amplitude of the main and one trailing signal for these elements were recorded.

5.3.2 Transfer Characteristics

The array's transfer characteristics were measured with the automatic test console. The data was recorded on magnetic tape and the tape later was processed by a computer.

The array response was measured at dark and at 15 preselected calibrated light levels. Integration time was 2 msec and the light intensity was changed by a combination of neutral density filter and variation of the distance between the array and light source, as described in paragraph 5.2.1. The calibrated irradiance levels were selected from Table 5-1.

To minimize the effect of DC drift in the instrumentation, two measurements were taken at each optical bench position. First, the array's dark response was recorded. The light response measurement followed immediately. The difference between the dark and light response was computed as the output signal. The output of each element of the array was recorded 99 times at each dark and light level.

The computer printout resulting from this test provided the information for deriving the array uniformity at dark and highlight and the linearity of the array's response.

5.3.3 Noise Characteristics

The system noise at each light level is calculated by the computer from the readings taken during the transfer characteristics test. This calculated noise includes the array noise as well as the noise contributed by the external video amplifier. and the A/D converter's quantizing noise.

A separate noise measurement was taken with an oscilloscope at the output of the external video amplifier. The peak to peak noise of the array-video amplifier combination was displayed on the oscilloscope screen and photographed. The RMS noise is 1/6 of the displayed peak to peak noise.

5.3.4 Spectral Response

The array spectral response was measured by illuminating the array with monochromatic light using the calibrated narrow band filters (see paragraph 5.2.2). The output of a typical array element was displayed on an oscilloscope and its signal amplitude was recorded for each irradiance band tested. The signal amplitude is defined as the difference between the element's output at dark and the output of the illuminated element. The measurement was taken at 9 wavelengths and under the conditions listed in Table 5-2.

5.3.5 Crosstalk and Element Profile

The crosstalk and element profile measurements were performed with the aid of the light probe. A monochromatic light spot, about 5 μm in diameter in the visible spectrum, was generated by placing the narrow band filters described in paragraph 4.2.3.2 in the probe's light path. Only four of these filters produced sufficient illumination to enable these measurements. The center wavelengths of these filters are:

$$\lambda_1 = 0.5893\ \mu m$$

$$\lambda_2 = 0.6708\ \mu m$$

$$\lambda_3 = 0.7670\ \mu m$$

$$\lambda_4 = 0.9000\ \mu m$$

In the visible band, the light spot was focused visually. In the longer wavelength, the spot was focused visually prior to the insertion of the filter, and then fine focused by peaking the signal observed on the oscilloscope.

5.3.5.1 Element Profile

The monochromatic light spot was positioned on the aluminum mask. The spot was scanned across element number 10 of the array, starting from the mask over the odd transport register and ending at the mask over the even transport register. The scanning was achieved by moving the array with the light probes X-Y stage in the X direction. The signal amplitude of element number 10 was recorded at 0.0001" increments for each wavelength.

5.3.5.2 Crosstalk

To measure the element to element crosstalk in the CCLID at different wavelengths, the monochromatic light spot was positioned at the center of element number 10, and the signal amplitude of the illuminated element (No. 10) and two adjacent elements (No. 8 and No. 9) were recorded. The output of the adjacent elements on the other side (No. 11 and No. 12) were ignored for this test, since they contained charge components accumulated due to transfer inefficiency as well as crosstalk.

A continuous scan along 5 array elements was performed at one wavelength (λ=.767 µm), and the output of the center element was recorded every 0.0001 inches. The Resulting reading provided a continuous plot of crosstalk versus position along the array.

5.3.6 Temperature

The array was held at a constant temperature while its response was recorded at dark and 15 preselected light levels, as in the transfer characteristics test (see paragraph 5.3.2). The temperature was controlled with a thermoelectric device (see paragraph 4.3).

The test was performed at three temperatures:

$$T_1 = 15°C$$

$$T_2 = 20°C$$

$$T_3 = 25°C$$

Lower temperature tests were attempted, but condensation and icing of the CCLID's glass window and electrical connections interfaced with both optical and electrical test conditions, producing false results.

5.3.7 Dark Current

The array's response due to dark current was measured at an increased integration time of 4 msec instead of the standard time of 2 msec. The average, minimum and maximum signal voltage caused by dark current was recorded. The signal voltage at saturation was also recorded.

SECTION 6

TEST RESULTS

6.1 GENERAL

This section describes the test results and the methods used in reducing these results into the reported form.

6.2 CHARGE TRANSFER EFFICIENCY

The procedure for measuring the charge transfer efficiency is described in paragraph 5.3.1. The test data contains the amplitudes of the main (M_i) and trailing (T_i) pulses for elements at the beginning and end of the array.

The ratio of $\frac{\sum T_i}{M_i + \sum T_i}$ represents the charge transfer inefficiency of the measured element. However, it contains losses incurred during transfers from the vertical to the horizontal register, and through the horizontal register to the array output. The inefficiency in the vertical transport registers of the linear CCI, is the difference between the inefficiencies of two elements, divided by the number of transfers between them.

$$\epsilon = \frac{1}{3N/2}\left(\frac{\sum T_{(i+N)}}{M_{(i+N)} + \sum T_{(i+N)}} - \frac{\sum T_i}{M_i + \sum T_i}\right)$$

Where N is the numerical separation between the tested elements and 3N is the number of transfers in the transport registers. Since the CCLID uses two transport registers, each register transports only half the elements of the array, and the number of transfers in each register is 3N/2. The transfer inefficiency is calculated for both odd and even registers, and hence, the transfer efficiencies of both registers are:

$$\eta_{odd} = 1 - \epsilon_{odd}$$

$$\eta_{even} = 1 - \epsilon_{even}$$

As an example, the transfer efficiency measurements for CCLID-500 S/N 31-4-2 at 0.5 saturation and a clocking rate of 250 KHz resulted with the following data:

$M_1 = 438.85$ mV	$T_{1A} = 7.26$ mV	$T_{1B} = 1.5$ mV
$M_{499} = 340.27$ mV	$T_{499A} = 9.53$ mV	$T_{499B} = 1.77$ mV
$M_2 = 363.28$ mV	$T_{2A} = 9.38$ mV	$T_{2B} = 1.31$ mV
$M_{500} = 301.74$ mV	$T_{500A} = 11.06$ mV	$T_{500B} = 2.04$ mV

The separation N is 500 elements. The number of transfers in each register is 750. The inefficiencies for each register are:

$$\epsilon_{odd} = \frac{1}{750}\left(\frac{9.53 + 1.77}{340.27 + 9.53 + 1.77} - \frac{7.26 + 1.5}{438.85 + 7.26 + 1.5}\right) = 0.000017$$

$$\epsilon_{even} = \frac{1}{750}\left(\frac{11.06 + 2.04}{301.74 + 11.06 + 2.04} - \frac{9.38 + 1.31}{363.28 + 9.38 + 1.31}\right) = 0.000016$$

The charge transfer efficiency for these registers is

$$\eta_{odd} = 1 - \epsilon_{odd} = 0.999983$$

$$\eta_{even} = 1 - \epsilon_{even} = 0.999984$$

The same array, at a light level of 25% of saturation showed almost identical charge transfer efficiency. At this light level

$$\eta_{odd} = 0.999971$$

$$\eta_{even} = 0.999982$$

For CCLID-60, the separation N is 56 and the number of transfer in each register is 84.

At 0.5 saturation and a clocking rate of 500 KHz, CCLID-60 S/N 62D-1-12 resulted with the following data:

$$M_3 = 208 \text{ mV} \qquad T_3 = 1 \text{ mV}$$
$$M_{57} = 203 \text{ mV} \qquad T_{57} = 3 \text{ mV}$$
$$M_4 = 202 \text{ mV} \qquad T_4 = 1 \text{ mV}$$
$$M_{58} = 198 \text{ mV} \qquad T_{58} = 3 \text{ mV}$$

$$\epsilon_{odd} = \frac{1}{84}\left(\frac{3}{206} - \frac{1}{209}\right) = 0.000116$$

$$\epsilon_{even} = \frac{1}{84}\left(\frac{3}{201} - \frac{1}{203}\right) = 0.000119$$

The transfer efficiency for this array is therefore,

$$\eta_{odd} = 0.999884$$
$$\eta_{even} = 0.999881$$

Table 6-1 lists the transfer efficiencies of the odd and even transport registers for the arrays tested. All tested arrays exhibited transfer efficiencies of approximately 99.99%. Obviously, the test results far exceed the instrumentation accuracy specifications. To increase the reading accuracy, each value for M_i and T_i was measured 6 times. The mean value of the 6 readings was used for the transfer efficiency calculation.

6.3 TRANSFER CHARACTERISTICS

The data recorded on tape during the transfer characteristics test (paragraph 5.3.2) is reduced by the computer in the following manner:

a) The mean output of each element at each light level is computed, based on the 99 readings per element taken during the test.

TABLE 6-1

CHARGE TRANSFER EFFICIENCY

S/N	Number of Elements	Clock Frequency (KHz)	Irradiance In % Sat.	η odd	η even
31-4-2	500	250	50	0.999983	0.999984
			25	0.999971	0.999982
62D-1-12	60	500	50	0.999884	0.999881
62D-1-13	60	500	50	0.999870	0.999913
62D-1-16	60	500	50	0.999951	0.999933
62D-1-28	60	500	50	0.999899	0.999896
62D-1-30	60	500	50	0.999944	0.999943

b) The mean output of each element at the dark test preceeding the corresponding light level is also computed.

c) The net signal for each element, consisting of the difference between the light and dark response is computed.

d) The RMS noise (σ) and the peak deviation below and above the computed mean are also calculated at dark and light.

This computed data is printed for each array element at each light level. Figure 6-1 is a sample printout of this data for elements 201 through 250 of CCLID 500 S/N 61A-2X-9 at light level #8, which for this test was 76 uJ/m^2.

After all the element data is computed at each light level, two composite tables are printed- the output response table and the signal response table.

The output response table lists the output of each array element at dark and at each light level tested. Figure 6-2 is a sample printout of the output response table for elements 201 through 250 of CCLID 500 S/N 61A-2X-9.

The signal response table lists the difference between the light and dark response of each array element at each light level tested. Figure 6-3 is a sample printout of the signal response table for elements 201 through 250 of CCLID 500 S/N 61A-2X-9.

The final computation results in the mean response of the whole array at each light level and the geometric mean of the RMS noise of all the array elements at each light level. Figure 6-4 shows the computer output for CCLID 500 S/N 61A-2X-9 listing these values.

In all computer printouts, the values are shown in bits, where each bit is equal to 4 m volts at the video amplifier output or 200 u volts at the array output. The linearity of response and the array uniformity was determined from the computer printout.

6.3.1 Linearity of Response

Figures 6-5 and 6-6 show the mean response curve of CCLID's S/N 61A-1-16 and 61A-2X-9 respectively. The ordinate shows the signal output at the arrays on-chip amplifier in volts. The abcissa represents the irradiance (E) in J/m^2.

LIGHT LEVEL 8

ELEMENT NUMBER	DARK	MEAN LIGHT	SIGNAL	DARK SIGMA	DEVIATION MIN	MAX	LIGHT SIGMA	DEVIATION MIN	MAX
201	28.0	60.7	32.7	0.0	0.0	0.0	1.0	0.7	1.3
202	26.1	58.4	32.3	0.4	0.1	1.9	0.9	2.4	1.6
203	28.0	63.3	35.2	0.3	0.0	2.0	1.0	1.3	0.7
204	26.1	63.4	37.3	0.4	0.1	1.9	1.4	1.4	1.6
205	28.1	64.5	36.5	0.3	0.1	1.9	0.5	0.5	0.5
206	26.7	69.0	42.3	1.0	0.7	1.3	0.6	1.0	5.0
207	28.1	61.3	33.2	0.3	0.1	1.9	0.6	1.3	0.7
208	27.5	55.2	27.7	0.9	1.5	0.5	2.7	3.2	2.8
209	28.3	57.9	29.7	0.7	0.3	1.7	0.6	5.9	0.1
210	26.4	51.1	24.7	0.8	0.4	1.6	1.0	1.1	0.9
211	28.0	52.2	24.1	0.3	0.0	2.0	1.0	0.2	5.8
212	26.1	57.4	31.4	0.3	0.1	1.9	1.7	5.4	0.6
213	28.0	62.7	34.7	0.0	0.0	0.0	1.0	0.7	2.3
214	26.0	61.2	35.2	0.2	0.0	2.0	1.0	1.2	0.8
215	28.0	60.8	32.8	0.0	0.0	0.0	1.0	0.8	1.2
216	26.0	60.4	34.4	0.2	0.0	2.0	0.8	0.4	1.6
217	28.0	58.0	30.0	0.0	0.0	0.0	0.2	0.0	2.0
218	26.2	62.7	36.5	0.5	0.2	1.8	1.0	0.7	2.3
219	28.0	59.1	31.1	0.2	0.0	2.0	1.0	1.1	1.9
220	26.1	62.4	36.2	0.5	0.1	1.9	0.8	0.4	2.6
221	28.0	64.3	36.3	0.0	0.0	0.0	0.6	0.3	1.7
222	26.1	58.3	32.1	0.5	0.1	1.9	0.4	0.3	0.7
223	28.0	64.5	36.5	0.3	0.0	2.0	0.8	0.5	1.5
224	26.1	59.7	33.6	0.4	0.1	1.9	0.8	1.7	1.3
225	28.1	57.9	29.8	0.3	0.1	1.9	0.9	5.9	1.1
226	26.2	58.1	31.9	0.5	0.2	1.8	0.5	0.1	1.9
227	28.0	58.1	30.1	0.0	0.0	0.0	0.5	0.1	1.9
228	26.0	60.3	34.3	0.3	0.0	2.0	0.7	0.3	1.7
229	28.0	60.7	32.7	0.0	0.0	0.0	1.0	0.7	1.3
230	26.0	62.1	36.1	0.0	0.0	0.0	0.3	0.1	1.9
231	28.0	62.0	34.0	0.0	0.0	0.0	0.2	2.0	0.0
232	26.0	60.6	34.6	0.0	0.0	0.0	0.9	0.6	1.4
233	28.0	59.9	32.0	0.2	2.0	0.0	0.3	1.9	0.1
234	26.0	59.2	33.2	0.0	0.0	0.0	1.0	1.2	0.8
235	28.0	60.0	32.0	0.2	2.0	0.0	0.3	2.0	0.0
236	26.0	63.7	37.7	0.2	0.0	2.0	0.7	1.7	0.3
237	28.0	62.0	34.0	0.2	2.0	0.0	0.3	1.0	3.0
238	26.1	63.6	37.5	0.3	0.1	1.9	0.9	1.6	1.4
239	28.0	64.8	36.8	0.0	0.0	0.0	0.4	0.8	0.2
240	26.1	60.9	34.8	0.5	0.1	1.9	0.4	0.9	1.1
241	28.0	62.4	34.4	0.0	0.0	0.0	1.0	0.4	2.6
242	26.1	62.0	35.9	0.3	0.1	1.9	0.4	2.0	3.0
243	28.0	62.0	34.0	0.0	0.0	0.0	0.4	2.0	2.0
244	26.0	61.8	35.8	0.0	0.0	0.0	0.6	1.8	0.2
245	28.0	62.6	34.6	0.0	0.0	0.0	0.9	0.6	1.4
246	26.0	62.0	35.9	0.2	0.0	2.0	0.3	2.0	0.0
247	28.0	63.6	35.6	0.3	2.0	2.0	0.8	1.6	0.4
248	26.0	62.0	35.9	0.2	0.0	2.0	0.2	1.0	0.0
249	28.0	61.3	33.3	0.0	0.0	0.0	1.0	1.3	0.7
250	26.0	61.7	35.7	0.0	0.0	0.0	0.7	1.7	0.3

FIGURE 6-1 SAMPLE COMPUTER PRINTOUT- INDIVIDUAL ELEMENT DATA

OUTPUT RESPONSE TABLE

ELEMENT NUMBER	LIGHT LEVELS 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
201	28.0	28.0	28.0	28.4	30.9	34.0	33.9	42.0	60.7	93.0	172.4	227.2	315.3	348.2	473.1	498.5
202	26.1	27.6	28.0	28.1	28.3	29.5	34.0	36.0	58.4	93.0	179.8	235.9	321.2	361.8	492.2	498.5
203	28.0	28.0	28.1	30.4	33.4	34.0	34.0	42.0	63.3	98.5	185.7	242.7	329.0	368.6	497.4	498.5
204	26.1	27.7	28.0	28.2	29.2	29.6	34.0	42.0	63.4	94.2	183.7	242.8	330.3	369.7	500.1	498.5
205	28.0	28.0	28.3	31.9	34.0	34.0	34.0	42.4	64.5	94.8	178.5	234.5	321.1	358.8	496.9	498.5
206	26.8	28.0	28.0	29.1	29.4	31.7	34.0	42.1	69.0	110.5	193.4	249.6	346.4	382.1	507.5	499.5
207	28.0	28.1	29.2	33.6	34.0	33.8	34.2	42.7	61.3	89.5	162.7	213.3	298.1	330.0	453.1	498.5
208	27.6	28.0	28.3	29.5	31.9	33.6	34.2	42.7	55.2	76.9	163.0	222.5	316.1	352.0	488.8	498.5
209	28.0	28.4	32.1	33.9	33.8	33.5	34.6	42.0	57.9	74.8	154.1	209.4	292.5	328.3	457.3	498.5
210	26.4	27.9	28.0	28.3	28.4	29.3	34.0	34.4	51.1	77.4	162.0	217.2	305.8	340.4	471.2	498.5
211	28.0	28.0	28.7	30.1	32.6	34.0	34.0	35.7	52.2	94.1	180.0	237.7	323.7	362.3	491.3	498.5
212	26.1	27.0	27.7	29.0	28.1	28.3	33.8	34.2	57.4	92.1	178.7	235.8	321.8	361.8	490.6	498.5
213	28.0	28.0	28.0	28.0	28.0	29.9	34.0	39.0	62.7	91.9	170.3	226.1	313.4	345.4	474.1	498.5
214	25.9	26.2	26.7	27.6	27.9	28.0	34.0	36.5	61.2	91.8	177.0	234.2	321.4	361.7	492.5	498.5
215	28.0	28.0	28.0	28.0	28.7	33.8	34.0	42.0	60.8	86.9	163.6	219.8	304.7	337.8	466.6	499.5
216	26.1	27.6	28.0	28.0	28.2	29.9	33.7	41.0	60.4	92.6	179.7	239.0	330.7	370.9	505.7	498.5
217	28.0	28.0	28.0	28.5	30.4	33.9	33.8	41.3	58.0	84.3	164.7	220.7	311.0	347.0	488.0	498.5
218	26.3	27.7	28.0	28.1	28.8	30.1	33.8	38.4	62.7	104.0	192.2	254.0	348.1	382.1	510.0	498.5
219	28.0	28.0	28.0	28.5	31.7	34.0	33.8	39.4	59.1	90.3	167.0	220.4	309.1	345.9	479.0	498.5
220	26.3	27.6	28.0	28.1	29.1	29.7	34.0	42.1	62.4	91.7	180.6	242.3	334.9	376.1	510.0	498.5
221	28.0	28.0	28.0	28.2	29.2	33.9	33.9	42.0	64.3	113.4	196.8	253.6	348.6	382.1	510.0	498.5
222	26.2	27.7	28.0	28.1	28.2	29.5	34.0	35.0	58.3	85.3	171.5	229.2	320.7	358.5	495.6	498.5
223	28.0	28.1	29.0	33.7	34.0	34.0	35.0	46.4	64.5	92.7	175.0	232.4	320.0	355.9	491.8	498.5
224	26.1	27.5	28.0	28.5	29.3	29.6	33.8	33.4	59.7	90.4	176.7	236.6	329.8	370.3	494.3	498.5
225	28.0	28.0	28.9	33.6	34.0	34.0	34.0	39.4	57.9	85.4	169.8	225.9	316.9	350.2	488.4	498.5
226	26.5	27.8	28.0	28.3	29.0	29.2	34.0	36.5	58.1	93.2	181.4	243.3	337.0	378.0	510.1	498.5
227	28.0	28.0	28.2	29.3	31.6	34.0	34.0	37.7	58.1	89.2	170.9	228.5	320.0	354.2	499.5	499.5
228	26.1	26.9	27.7	28.0	28.1	29.0	34.0	37.0	60.3	97.1	190.0	252.5	347.6	382.0	510.0	498.5
229	28.0	28.0	28.0	28.0	28.4	33.8	34.0	41.1	60.7	92.3	181.3	242.4	335.8	376.1	510.0	498.5
230	26.0	26.9	27.8	28.0	28.0	29.1	34.0	41.4	62.1	92.3	179.6	238.7	330.8	370.6	506.5	498.5
231	28.0	28.0	28.0	28.0	28.7	33.9	34.0	42.0	62.0	91.1	177.5	235.9	328.2	366.9	509.7	498.5
232	26.1	27.4	28.0	28.0	28.1	29.9	34.0	41.8	60.6	90.5	180.6	243.6	337.6	378.1	510.0	499.5
233	28.0	28.0	28.0	28.1	30.4	34.0	34.0	42.0	59.9	90.3	170.0	224.4	313.2	347.1	482.0	498.5
234	26.0	27.3	28.0	28.0	28.7	29.4	34.0	36.0	59.2	98.4	186.6	244.1	335.8	375.7	510.0	498.5
235	28.0	28.0	28.0	28.6	31.4	33.9	34.0	41.7	60.0	91.1	176.9	235.8	328.8	367.2	509.6	498.5
236	26.1	26.9	27.8	28.0	28.4	29.5	34.0	39.1	63.7	96.9	189.8	251.3	352.0	383.2	510.0	498.5
237	28.0	28.0	28.0	28.2	29.7	34.0	34.0	41.9	62.0	98.6	188.6	247.1	340.1	375.3	510.0	498.5
238	26.1	27.3	28.0	28.0	28.4	29.6	34.0	42.1	63.6	90.9	181.7	244.0	340.8	375.6	510.0	498.5
239	28.0	28.0	28.0	28.4	31.0	34.0	34.0	42.1	64.8	94.0	178.4	236.3	324.5	362.9	504.5	498.5
240	26.3	27.8	28.0	28.2	28.9	30.6	34.0	38.0	60.9	97.1	185.7	243.2	334.3	373.9	509.6	498.5
241	28.0	28.0	28.1	30.4	33.7	34.0	34.0	42.1	62.4	94.2	180.8	240.0	328.9	367.3	507.6	498.5
242	26.1	27.3	28.0	28.2	29.0	29.5	34.0	40.4	62.0	94.0	183.4	243.2	336.5	376.2	509.8	498.5
243	28.0	28.0	28.0	29.8	32.9	34.0	34.0	42.0	62.0	94.1	177.2	233.1	320.1	354.2	504.8	498.5
244	26.0	27.3	28.0	28.2	28.7	29.2	34.0	41.9	61.8	94.1	189.5	253.6	354.0	384.0	510.0	498.5
245	28.0	28.0	28.0	28.2	29.2	34.0	34.0	42.0	62.6	95.6	184.5	242.8	334.1	372.6	510.0	498.5
246	26.1	26.9	27.8	28.0	28.1	29.2	34.0	41.4	62.0	96.4	190.1	254.0	353.1	383.9	510.0	498.5
247	28.0	28.0	28.0	28.1	30.4	34.0	34.0	42.0	63.6	95.5	186.5	247.0	340.6	371.2	510.0	498.5
248	26.0	26.8	27.8	28.0	28.3	29.5	34.0	41.2	62.0	94.2	186.4	248.4	341.8	371.7	510.0	498.5
249	28.0	28.0	28.1	29.3	32.9	34.0	34.0	42.0	61.3	93.8	184.9	244.8	340.9	376.6	510.0	499.5
250	26.1	27.4	28.0	28.2	29.2	29.8	34.0	41.6	61.7	96.7	186.1	245.4	339.3	375.7	510.0	498.5

FIGURE 6-2 SAMPLE COMPUTER PRINTOUT-OUTPUT RESPONSE TABLE

SIGNAL RESPONSE TABLE

ELEMENT NUMBER	LIGHT LEVELS 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
201	0.0	0.0	0.0	0.4	2.9	6.0	5.9	14.0	32.7	65.0	144.4	199.2	287.3	320.2	445.1	470.5
202	0.0	1.5	1.7	1.6	2.1	3.4	7.7	9.7	32.3	67.0	153.6	209.8	295.2	335.7	466.2	472.4
203	0.0	0.0	0.1	2.4	5.4	6.0	5.0	14.0	35.2	70.5	157.7	214.7	301.0	340.5	469.4	470.5
204	0.0	1.6	1.7	1.8	2.8	3.1	7.7	15.7	37.3	67.9	157.6	216.7	304.3	343.7	474.1	472.5
205	0.0	0.0	0.3	3.9	6.0	6.0	5.0	14.4	36.5	66.7	150.4	206.5	293.0	330.8	468.8	470.5
206	0.0	1.2	1.1	1.9	2.3	4.9	7.2	15.3	42.3	83.9	166.9	223.0	319.9	355.7	481.2	472.2
207	0.0	0.1	1.2	5.6	6.0	5.7	5.2	14.6	33.2	61.4	134.7	185.2	270.1	302.0	425.1	470.4
208	0.0	0.4	0.5	1.6	4.3	5.9	6.5	15.0	27.7	49.3	135.7	195.1	288.9	324.8	461.8	471.5
209	0.0	0.4	4.1	5.9	5.8	5.3	5.4	13.8	29.7	46.4	125.8	181.1	264.2	300.0	428.9	470.1
210	0.0	1.5	1.3	1.5	1.8	2.7	7.4	7.6	24.7	51.1	135.7	190.9	279.4	314.2	445.0	472.3
211	0.0	0.0	0.7	2.1	4.6	5.9	5.0	7.7	24.1	66.1	152.0	209.6	295.6	334.2	463.3	470.4
212	0.0	0.9	1.6	1.8	1.8	2.1	7.6	8.0	31.4	66.0	152.6	209.7	295.8	335.8	464.5	472.5
213	0.0	0.0	0.0	0.0	0.0	1.9	5.0	11.0	34.7	63.9	142.3	198.1	285.4	317.4	446.1	470.6
214	0.0	0.3	0.7	1.6	1.9	2.0	8.0	10.5	35.2	65.8	151.0	208.2	295.4	335.7	466.5	472.5
215	0.0	0.0	0.0	0.0	0.7	5.8	5.0	14.0	32.8	58.9	135.6	191.9	276.7	309.8	438.6	470.5
216	0.0	1.5	2.0	1.9	2.1	3.8	7.6	14.9	34.4	66.6	153.7	213.0	304.7	344.9	479.7	472.5
217	0.0	0.0	0.0	0.5	2.4	5.9	5.8	13.3	30.0	56.3	136.7	192.7	283.0	319.0	460.0	470.5
218	0.0	1.5	1.6	1.8	2.5	3.7	7.6	12.1	36.5	77.8	166.0	227.9	322.0	356.0	483.9	472.4
219	0.0	0.0	0.0	0.5	3.7	5.9	5.8	11.4	31.1	62.3	139.0	192.4	281.1	317.9	451.0	470.5
220	0.0	1.3	1.7	1.5	3.0	3.5	7.6	15.8	36.2	65.4	154.6	216.2	308.9	350.1	484.0	472.5
221	0.0	0.0	0.0	0.2	1.2	5.9	5.9	14.0	36.3	85.4	168.9	225.6	320.6	354.1	482.1	470.6
222	0.0	1.4	1.7	1.6	1.9	3.2	7.8	9.8	32.1	59.2	145.5	203.2	294.7	332.5	469.6	472.5
223	0.0	0.1	1.0	5.7	6.0	5.9	7.9	18.3	36.5	64.6	147.0	204.3	292.0	327.9	463.7	470.5
224	0.0	1.4	1.8	2.3	3.2	3.5	7.7	12.1	33.6	64.4	150.7	210.6	303.8	344.3	468.2	472.4
225	0.0	0.0	0.9	5.6	5.9	5.9	5.9	11.2	29.8	57.3	141.8	197.7	288.8	322.0	460.3	470.4
226	0.0	1.3	1.6	1.8	2.6	2.8	7.7	10.2	31.9	67.1	155.3	217.2	310.9	351.9	484.0	472.4
227	0.0	0.0	0.2	1.3	3.6	6.0	5.0	9.7	30.1	61.2	142.9	200.5	292.0	326.2	471.5	470.5
228	0.0	0.8	1.7	1.8	2.0	2.9	7.9	10.9	34.3	71.1	164.0	226.5	321.6	356.0	484.0	472.5
229	0.0	0.0	0.0	0.0	0.4	5.8	5.0	13.1	32.7	64.3	153.3	214.4	307.8	348.1	482.0	470.5
230	0.0	0.9	1.8	1.8	2.0	3.1	8.0	15.4	36.1	66.3	153.6	212.7	304.8	344.6	480.5	472.5
231	0.0	0.0	0.0	0.0	0.7	5.9	5.0	14.0	34.0	63.1	149.5	207.9	300.2	339.0	481.8	470.5
232	0.0	1.3	1.9	1.9	2.0	3.8	7.9	15.8	34.6	64.5	154.6	217.6	311.6	352.1	483.9	472.5
233	0.0	0.0	0.0	0.1	2.4	6.0	5.0	14.0	32.0	62.3	142.0	196.4	285.2	319.1	454.1	470.6
234	0.0	1.3	1.9	1.9	2.6	3.3	7.9	9.9	33.2	72.4	160.6	218.1	309.8	349.7	484.0	472.5
235	0.0	0.0	0.0	0.6	3.4	5.9	5.0	13.7	32.0	63.1	148.9	207.8	300.8	339.3	481.7	470.5
236	0.0	0.8	1.8	1.9	2.4	3.5	7.9	13.1	37.7	70.9	163.8	225.3	326.0	357.2	484.0	472.5
237	0.0	0.0	0.0	0.2	1.7	6.0	5.0	13.9	34.0	70.6	160.6	219.1	312.1	347.3	482.1	470.5
238	0.0	1.2	1.9	1.9	2.2	3.6	8.0	16.0	37.5	64.9	155.7	218.0	314.8	349.6	484.0	472.5
239	0.0	0.0	0.0	0.4	3.1	6.0	5.0	14.1	36.8	66.0	150.5	208.3	296.5	334.9	476.5	470.5
240	0.0	1.5	1.7	1.7	2.6	4.3	7.8	11.8	34.0	71.0	159.6	217.1	308.2	347.9	483.5	472.5
241	0.0	0.0	0.1	2.4	5.7	5.9	5.0	14.1	34.4	66.2	152.8	217.1	300.9	339.3	479.6	470.5
242	0.0	1.2	1.8	2.0	2.9	3.5	7.9	14.4	35.9	68.0	157.4	217.2	310.5	350.2	483.8	472.5
243	0.0	0.0	0.0	1.8	4.9	6.0	5.0	14.0	34.0	66.1	149.2	205.1	292.1	326.2	476.8	470.5
244	0.0	1.3	1.9	2.0	2.5	3.1	8.0	15.9	35.8	68.1	163.5	227.6	328.0	358.0	484.0	472.5
245	0.0	0.0	0.0	0.2	1.2	6.0	5.0	14.0	34.6	67.6	156.5	214.9	306.1	344.6	482.0	470.5
246	0.0	0.8	1.8	2.0	2.0	3.1	8.0	15.4	35.9	70.4	164.1	228.0	327.1	357.9	484.0	472.5
247	0.0	0.0	0.0	0.1	2.4	6.0	5.0	14.0	35.6	67.5	158.5	219.1	312.6	343.3	482.1	470.6
248	0.0	0.8	1.8	2.0	2.3	3.4	8.0	15.2	35.9	68.2	160.4	222.4	315.8	345.6	484.0	472.5
249	0.0	0.0	0.1	1.3	4.9	6.0	5.0	14.0	33.3	65.8	156.9	216.8	312.9	348.6	482.0	470.5
250	0.0	1.3	1.9	2.0	3.1	3.5	7.9	15.6	35.7	70.7	160.1	219.4	313.3	349.7	484.0	472.5

FIGURE 6-3 SAMPLE COMPUTER PRINTOUT-SIGNAL RESPONSE TABLE

CCD 500A NO. 61-A-2X-9 OCT 24,1972 TRANSFER CHARACTERISTICS, ROOM TEMPERATURE

LIGHT LEVELS

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MEAN	0.0	0.5	1.0	1.8	2.6	4.3	6.7	12.6	32.9	64.1	146.6	202.8	291.1	325.8	453.7	473.3
RMS NOISE	1.17	0.76	0.94	1.13	1.34	1.24	0.44	1.20	0.87	1.16	1.40	2.22	1.52	2.00	2.64	6.37

FIGURE 6-4 COMPUTER PRINTOUT-MEAN ARRAY RESPONSE

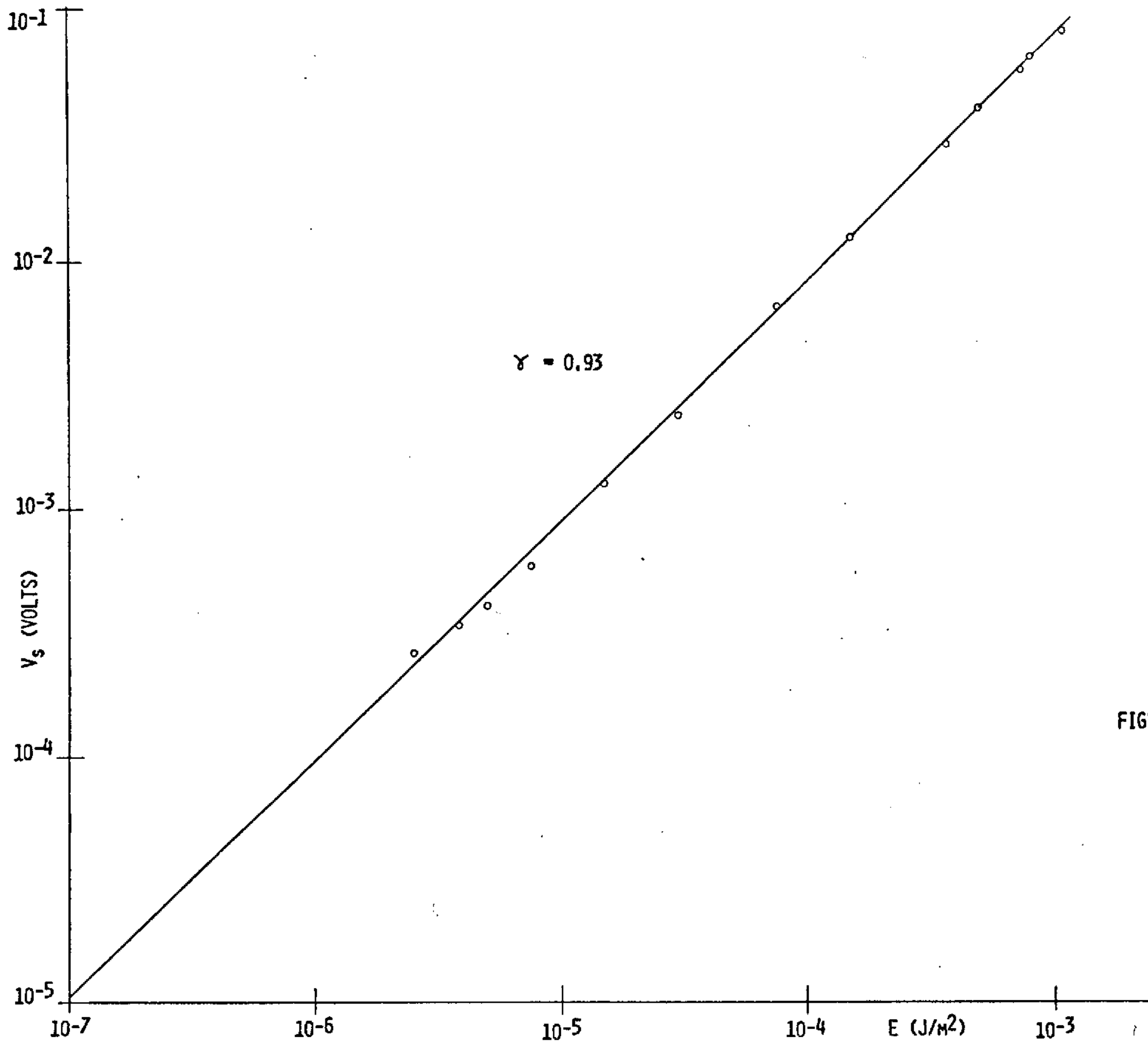


FIGURE 6-5 SIGNAL TRANSFER CURVE
FOR CCLID 500 S/N 61A-1-16

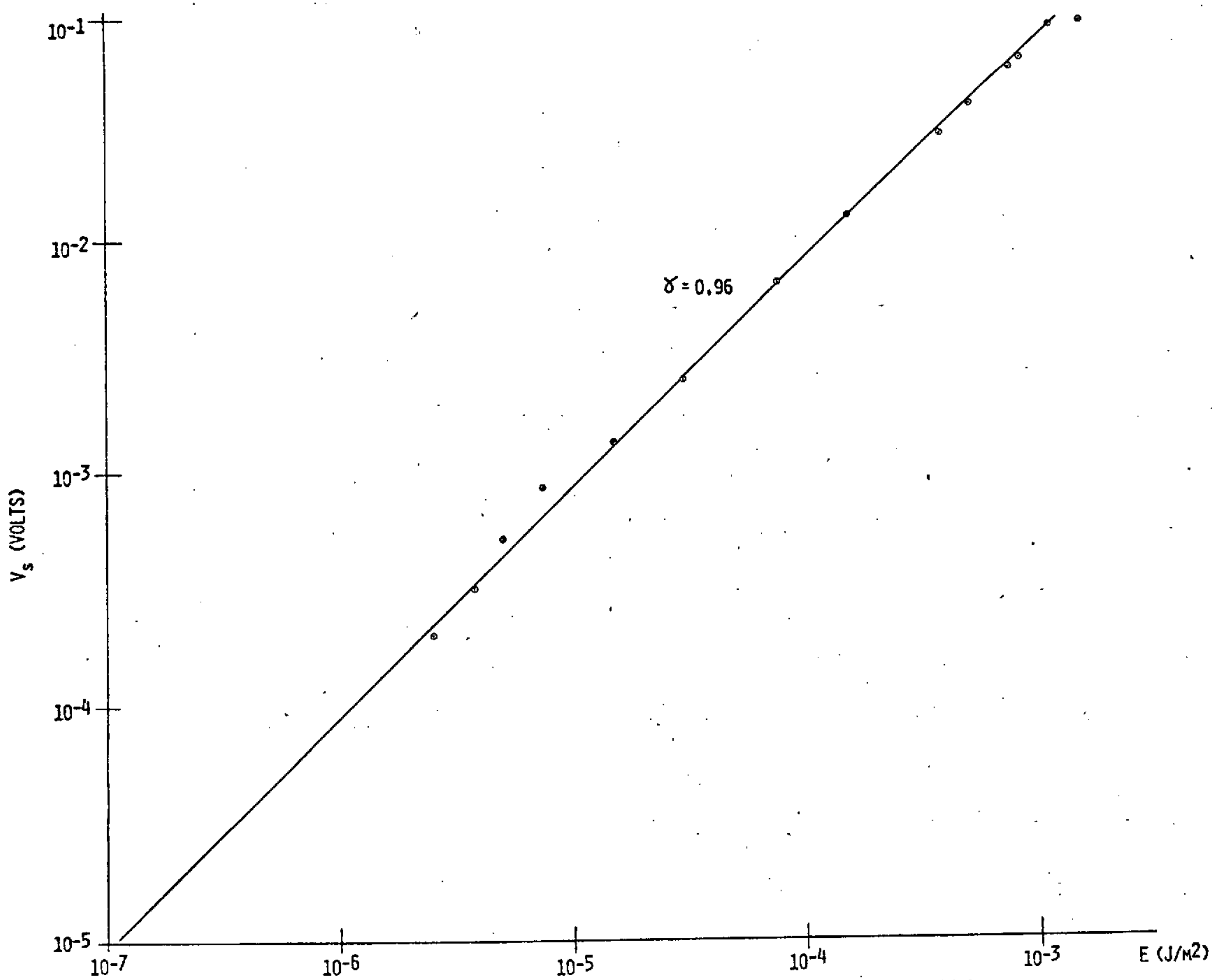


FIGURE 6-6 SIGNAL TRANSFER CURVE FOR CCLID 500 S/N 61A-2X-9

Both arrays exhibit an exponential response curve

$$V = KE^{\gamma}$$

For CCLID 500 S/N 61A-1-16

$$\gamma = 0.93$$

For CCLID 500 S/N 61A-2X-9

$$\gamma = 0.96$$

6.3.2 Uniformity of Response

The computer generated output response table (see figure 6-2) provided the basic data for analizing the uniformity of the CCLID response at different light levels. Figure 6-7 shows the response of all the elements of CCLID 500 S/N 61A-2X-9 at low, medium and high light levels. The plot is on semi-log paper, where the ordinate shows the video amplifier output in bits, where each bit equals 4 mV, and the abcissa shows the element number. Figure 6-8 shows a multiple exposure photograph of an oscilloscope screen showing the response at dark and three light levels of CCLID 500 S/N 61A-2X-9. On this photograph, the top trace shows the array response at dark. The second trace from the top is the array response at 250 uJ/m^2, the third is at 500 uJ/m^2 and the bottom trace is near saturation, at 1134 uJ/m^2.

Both figures show two types of non uniformities - one is a slowly varying non-uniformity along the array and the other is an element to element variation. The slow variation is attributed to the semiconductor process control and to the uneven layers of opaque paint covering the bulk silicon. The element to element variation consists of an odd-even pattern, and is attributed to non-uniform transfers into and out of the odd and even transport registers. Both types of non-uniformities have been reduced in later chips.

Figures 6-9 and 6-10 show the change in non-uniformity with light level for the two CCLIDs. The upper curve in each figure is the peak non-uniformity in percent of saturation signal. The lower curve shows the standard deviation from the mean, in percent of saturation signal.

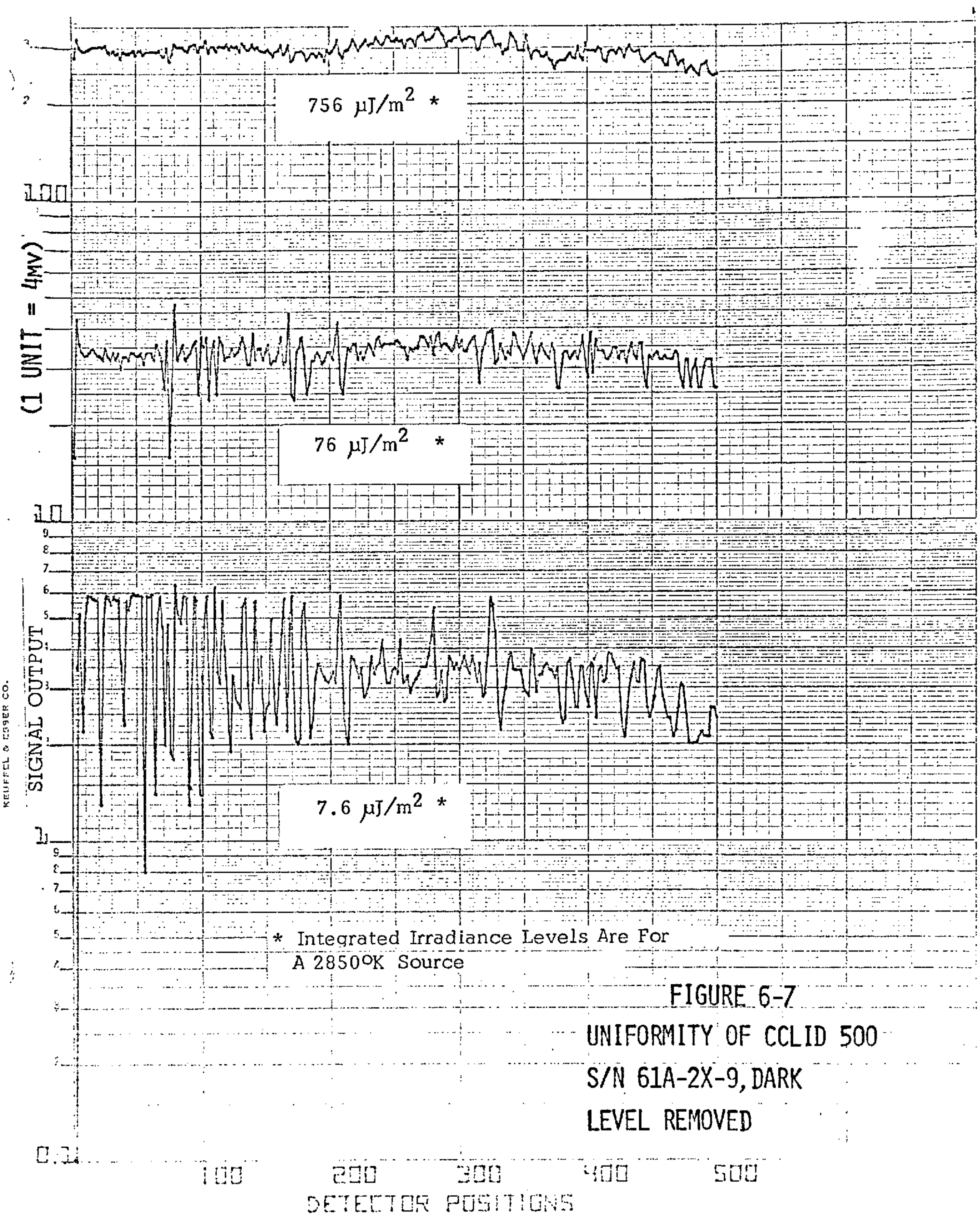


FIGURE 6-7
UNIFORMITY OF CCLID 500
S/N 61A-2X-9, DARK
LEVEL REMOVED

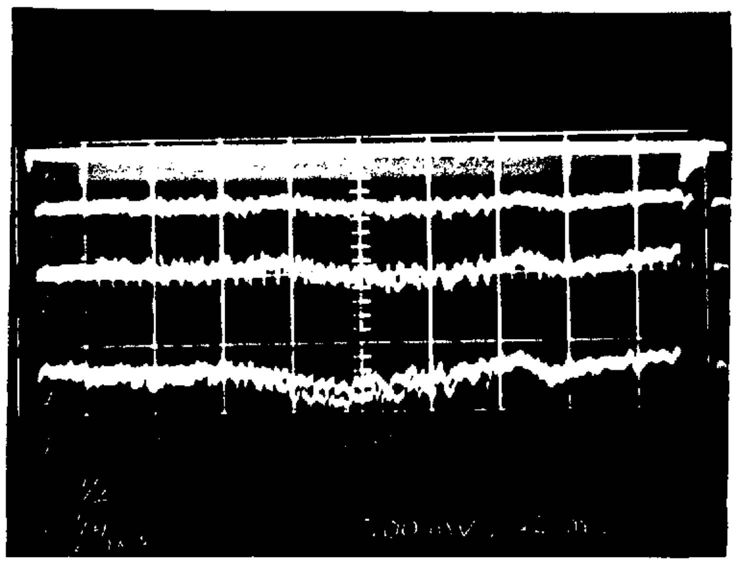


FIGURE 6-8: ARRAY UNIFORMITY

SCALE: Y = 500 mV/Box
X = 2 ms/Box

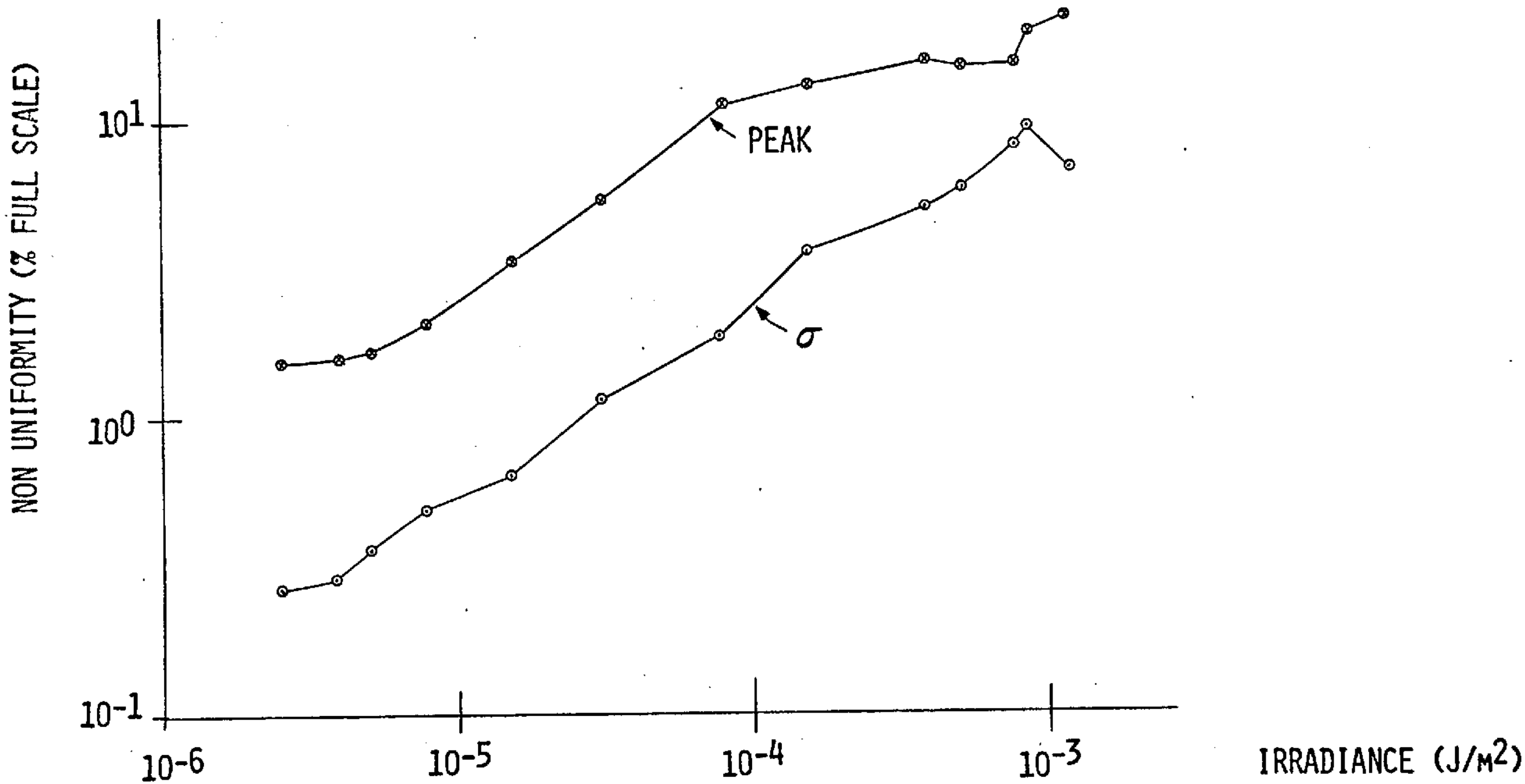


FIGURE 6-9 NON UNIFORMITY Vs. IRRADIANCE FOR CCLID 500 S/N 61A-1-16

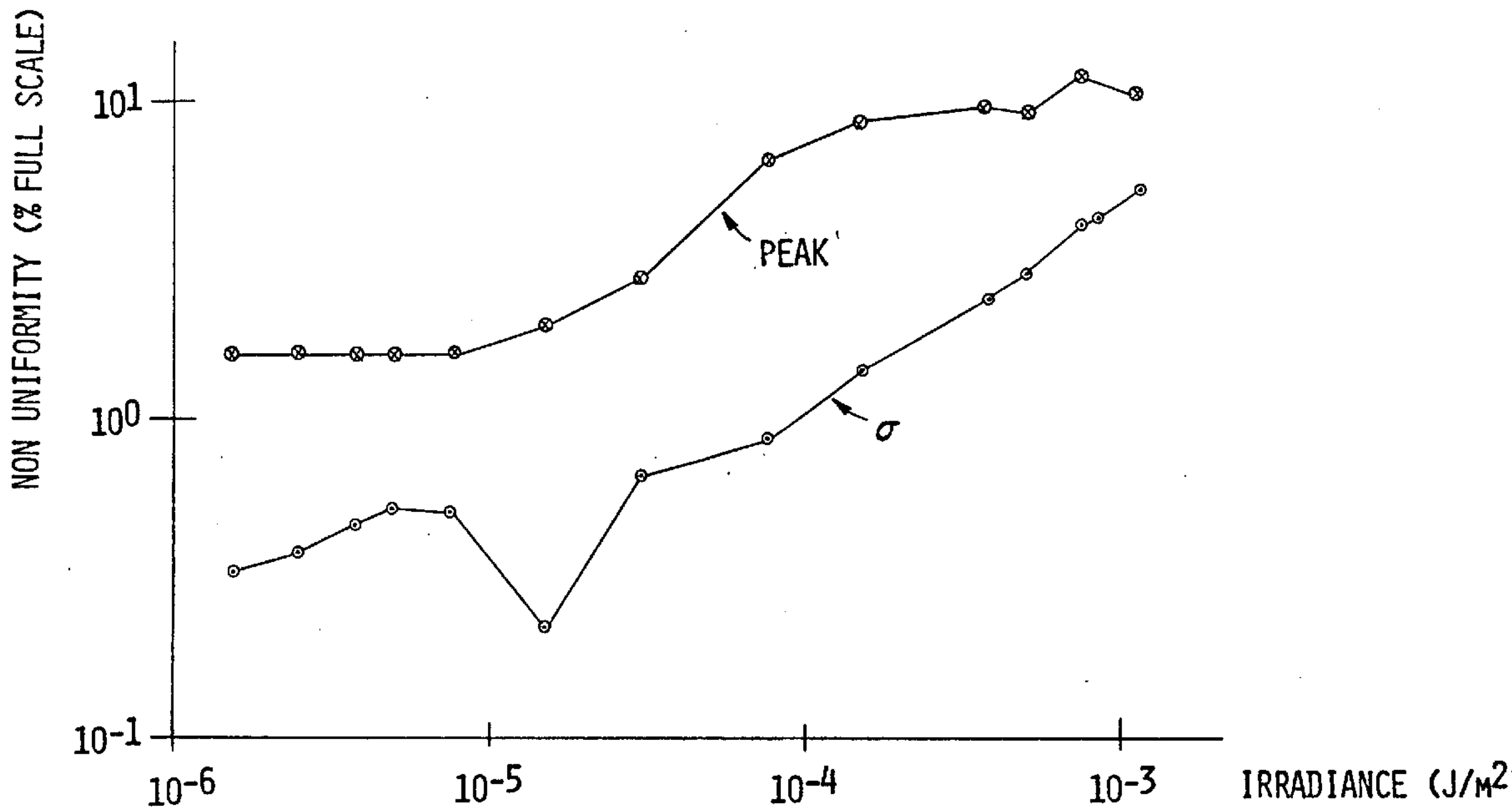


FIGURE 6-10 NON UNIFORMITY Vs. IRRADIANCE FOR CCLID 500 S/N 61A-2X-9

6.4 NOISE CHARACTERISTICS

The test system's noise characteristics was obtained during the transfer characteristics test and calculated by the computer. To isolate the array noise from the system noise, the output of individual array elements was displayed on an oscilloscope at a vertical scale of 2 mV/cm. The horizontal scale was adjusted to contain the output of just one array element on the scope screen. Several array elements were measured for both CCLID 500 S/N 61A-1-16 and S/N 61A-2X-9, with the array at dark. All measured elements displayed the same amount of noise

$$V_{n\,p\text{-}p} = 3 \text{ mV}$$

at the output of the amplifier. Figure 6-11 is a photograph of the noise generated by element number 214 of CCLID 500 S/N 61A-2X-9.

To find the noise at the output of the array, $V_{n\,p\text{-}p}$ is divided by the gain of the video amplifier. The array peak to peak noise is therefore

$$V_{nA} = \frac{3.10^{-3}}{20} = 150 \ \mu\text{V}$$

The RMS noise is 1/6 of the peak to peak noise, and therefore equal to

$$V_{RMS} = \frac{150}{6} = 25 \ \mu\text{V}$$

The minimum detectable signal at 4:1 signal to noise ratio is therefore

$$V_{s\,min} = 4 \times 25 = 100 \ \mu\text{V}$$

The array's sensitivity is defined from the signal transfer curves, figures 6-5 and 6-6, as the irradiance required to produce a signal equal to $V_{s\,min}$. From the signal transfer curves, figures 6-5 and 6-6, the sensitivity of CCLID 500 S/N 61A-1-16 at an irradiance of 2850°K is

$$E_{min} = 1.03 \ \mu\text{J/m}^2$$

and for CCLID S/N 61A-2X-9

$$E_{min} = 1.2 \ \mu\text{J/m}^2$$

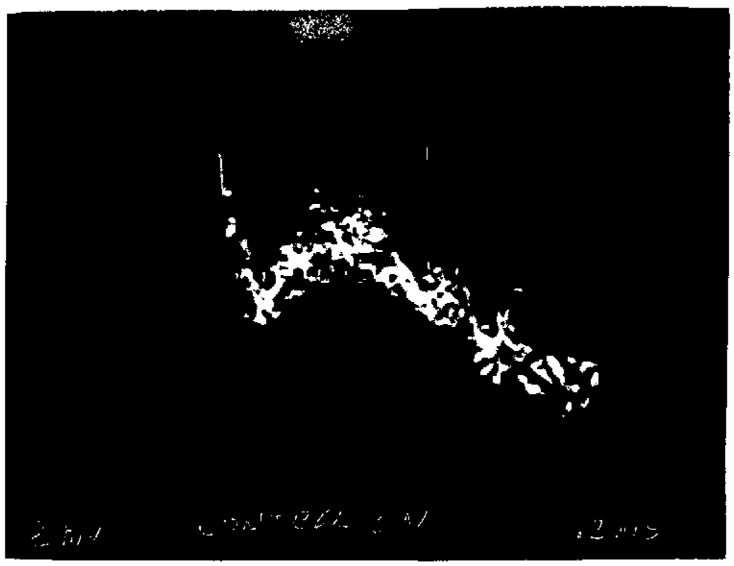


FIGURE 6-11: ARRAY NOISE AT DARK

SCALE: Y = 2mV/Box
X = 200 ns/Box

The CCLID's dynamic range is the ratio between the irradiance level required to saturate the array and the array's sensitivity

$$DR = \frac{E_{sat}}{E_{min}}$$

The saturation irradiance is again derived from the signal transfer curves. For both arrays,

$$E_{sat} = 1134\ \mu J/m^2$$

The dynamic range for CCLID 500 S/N 61A-1-16 is therefore

$$DR = \frac{1134}{1.03} = 1100:1$$

For CCLID 500 S/N 61A-2X-9

$$DR = \frac{1134}{1.2} = 945:1$$

The array noise increases with irradiance as shown in figure 6-12. The noise values in this curve are derived from the computed system RMS noise at each light level tested. The system noise is interpolated to provide the array noise, based on the oscilloscope noise measurement taken at dark.

6.5 SPECTRAL RESPONSE

The array's response to monochromatic light of different wavelengths was measured as described in paragraph 5.3.4. The irradiance level at each wavelength measured (I_{fi}) is known from table 5-2. The array signal response (V_λ) is measured. The spectral responsivity (K_λ) at each wavelength is

$$K_\lambda = \frac{V_\lambda}{I_{fi}}$$

The spectral response test was performed on CCLID 60 S/N 25-1-5. Table 6-2 lists the center wavelength of the filter used, the irradiance level at that wavelength, the signal output at the array's on-chip amplifier and the array responsivity. Figure 6-13 shows the spectral response curve for this array.

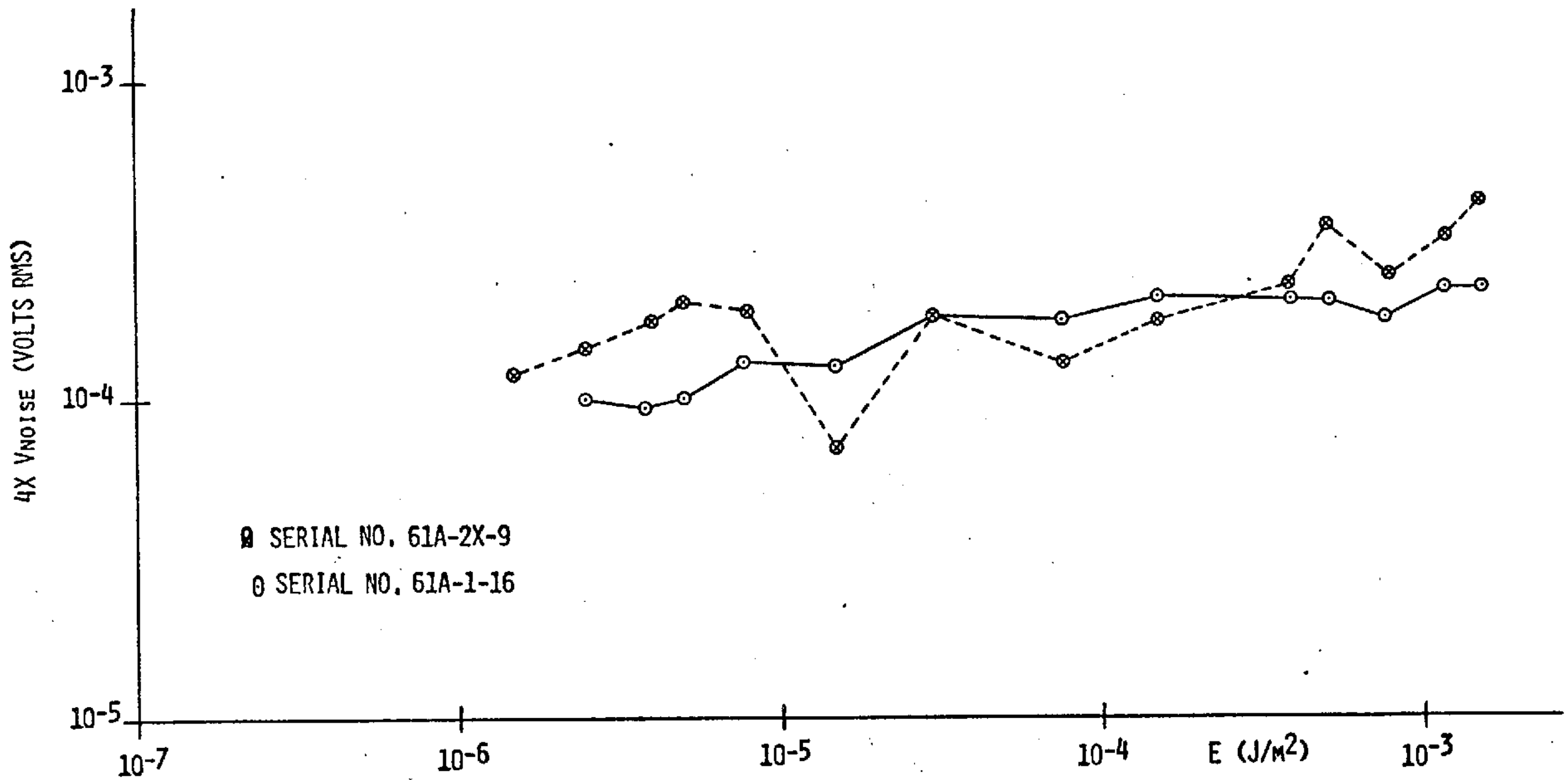


FIGURE 6-12 ARRAY NOISE CHARACTERISTICS

(INTERPOLATED FROM SYSTEM RMS NOISE)

TABLE 6-2

SPECTRAL RESPONSIVITY, CCLID-60 S/N 25-1-5

Center Wavelength (λ_c nm)	Test Irradiance (I_{fi} $\mu W/cm^2$)	Signal Output (V_λ mV)	Spectral Responsivity (K $\frac{mV}{\mu W/cm^2}$)
404.7	3.36	0.25	0.074
486.1	17.72	9.23	0.521
589.3	11.96	24.28	2.030
670.8	16.05	48.48	3.020
767.0	21.0	70.15	3.340
900.0	33.51	83.30	2.485
1014.0	95.0	75.65	0.796
1100.0	56.9	24.85	0.437
1200.0	65.9	0.50	0.008

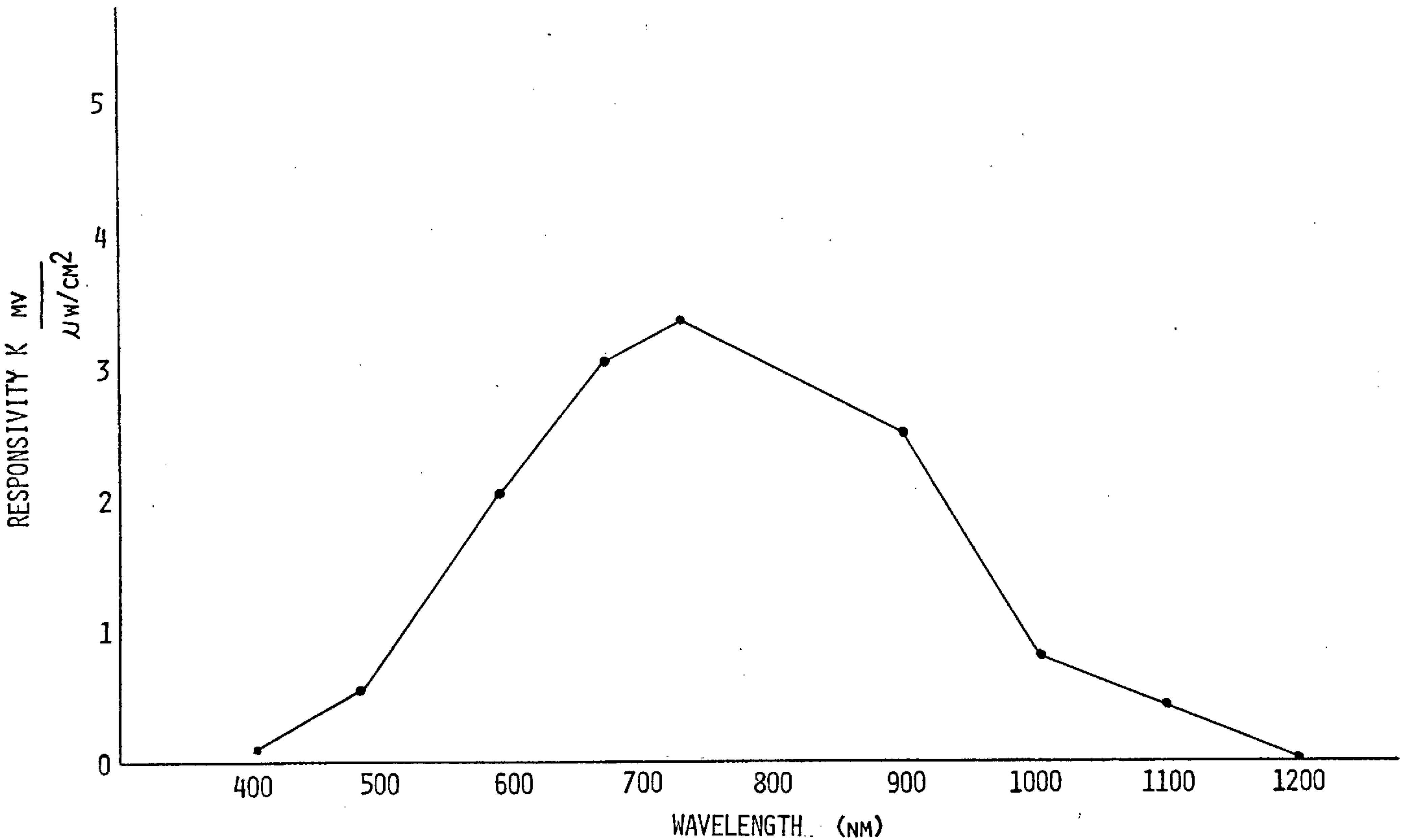


FIGURE 6-13 SPECTRAL RESPONSE CCLID 60 S/N 25-1-5

A spectral response measurement over a continuous silicon spectrum was performed at Fairchild R&D facility on CCLID 500 S/N 62B-W4-18. The spectral response curve for this array is shown in figure 6-14. The non uniform response is due to interference caused by the polysilicon gate layers which are deposited over the photoelements.

6.6 CROSSTALK AND ELEMENT PROFILE

The CCLID element profile was measured by passing a monochromatic light spot across an array element and recording the elements response. The profile of element number 10 of CCLID-60 S/N 25-1-5 was measured with monochromatic spots at 0.5893 μm, 0.6708 μm, 0.767 μm and 0.9 μm. Figures 6-15 through 6-18 show the normalized response of the measured elements.

Crosstalk was measured for the same wavelengths by centering the spot on the element and measuring its response and the response of the adjacent elements. Table 6-3 lists the wavelengths and crosstalk at adjacent elements in percent of the illuminated element output signal for CCLID 60 S/N 25-1-5.

A plot of continuous crosstalk response at .7670 μm is shown in figure 6-19. This plot shows the combined crosstalk - transfer efficiency effect on the right hand side, while the left hand side shows crosstalk effects only.

6.7 TEMPERATURE

The transfer characteristics of CCLID 500 S/N 61A-1-16 were measured under controlled array temperature at 15°C, 20°C and 25°C. Figure 6-20 shows the array's transfer curve at each of these temperatures. These curves show a slight increase in gamma with temperature.

6.8 DARK CURRENT

The signals generated in the CCLID due to dark currents were measured at an integration time of 4 msec. and the resulting measurements were linearly extrapolated into a 2 msec integration time.

TABLE 6-3

CROSSTALK, CCLID 60 S/N 25-1-5

WAVELENGTH µm	% CROSSTALK	
	1 ELEMENT AWAY	2 ELEMENTS AWAY
.5093	1.04	0.0
.6708	.96	0.0
.7670	8.41	0.93
.9000	7.18	0.77

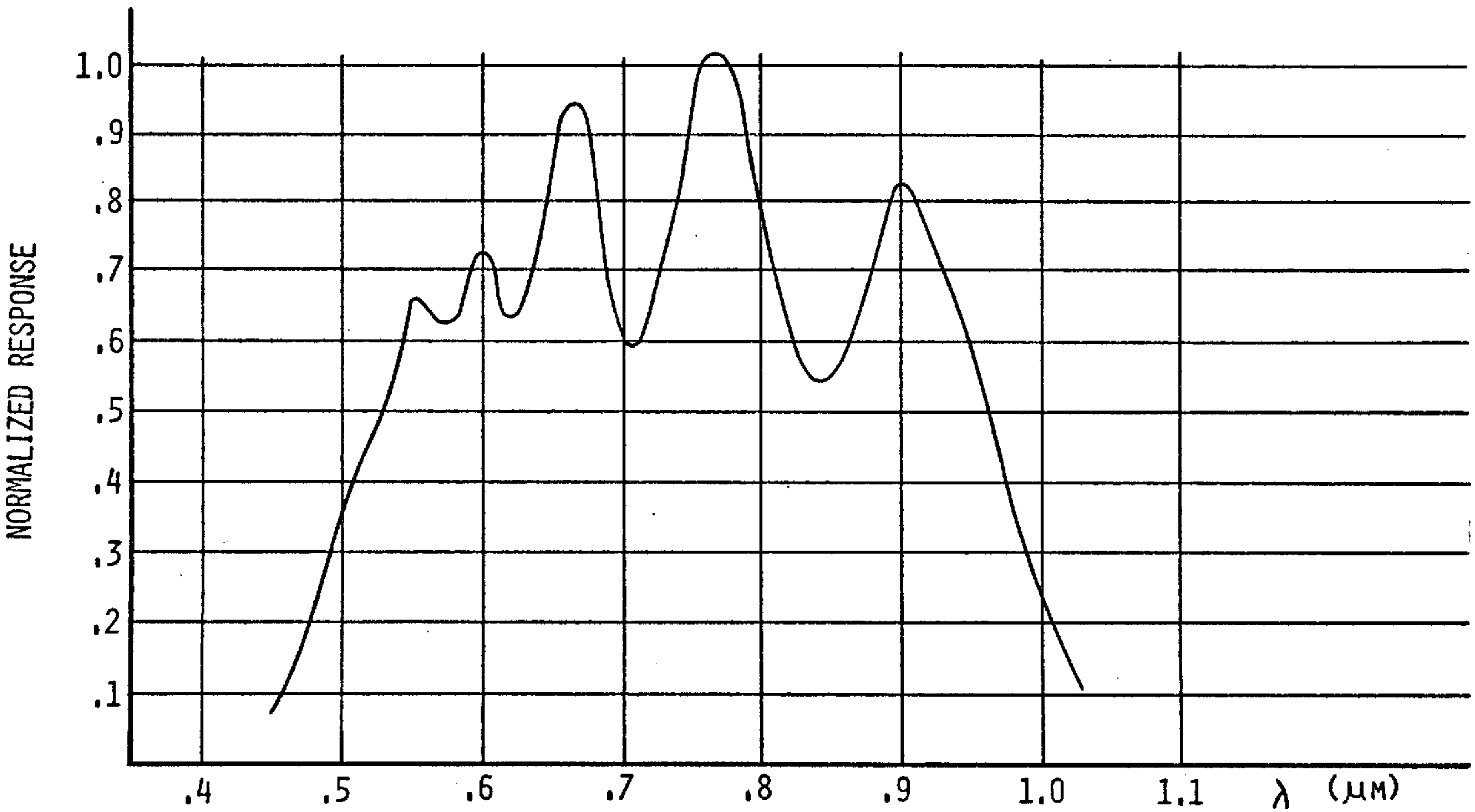


FIGURE 6-14 SPECTRAL RESPONSE CCLID 500 S/N 62B-W4-18

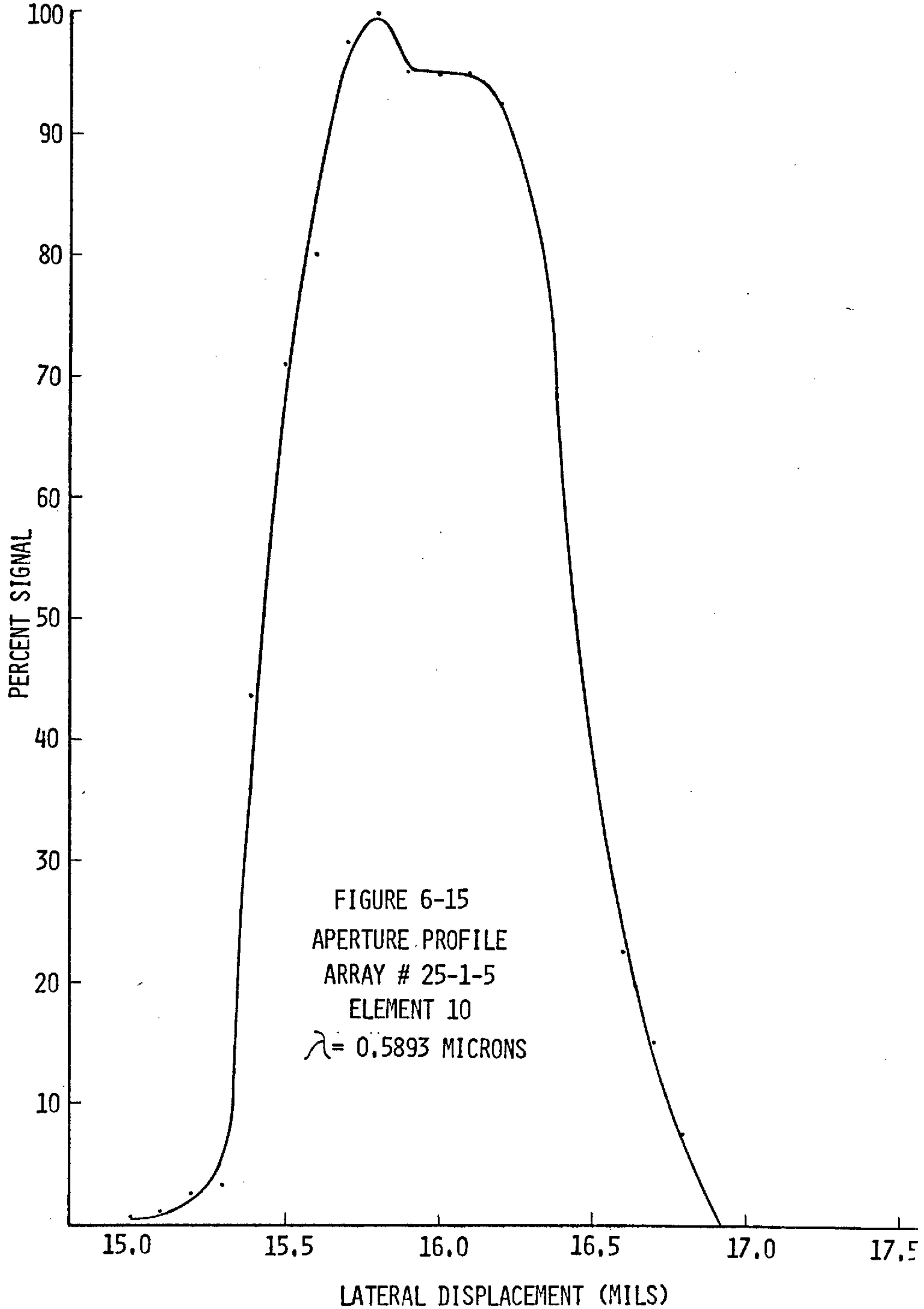


FIGURE 6-15
APERTURE PROFILE
ARRAY # 25-1-5
ELEMENT 10
λ= 0.5893 MICRONS

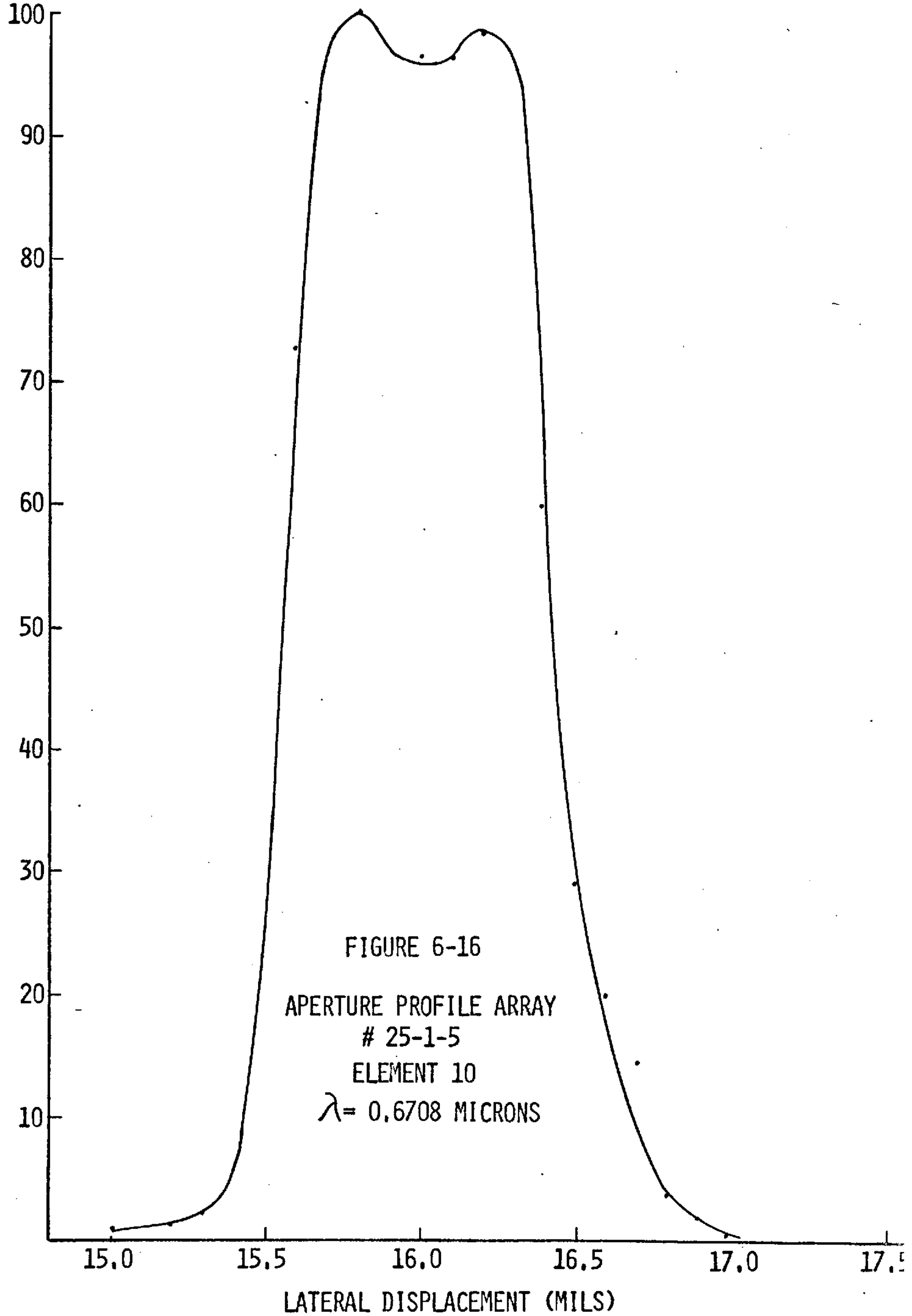


FIGURE 6-16

APERTURE PROFILE ARRAY
25-1-5
ELEMENT 10
λ= 0.6708 MICRONS

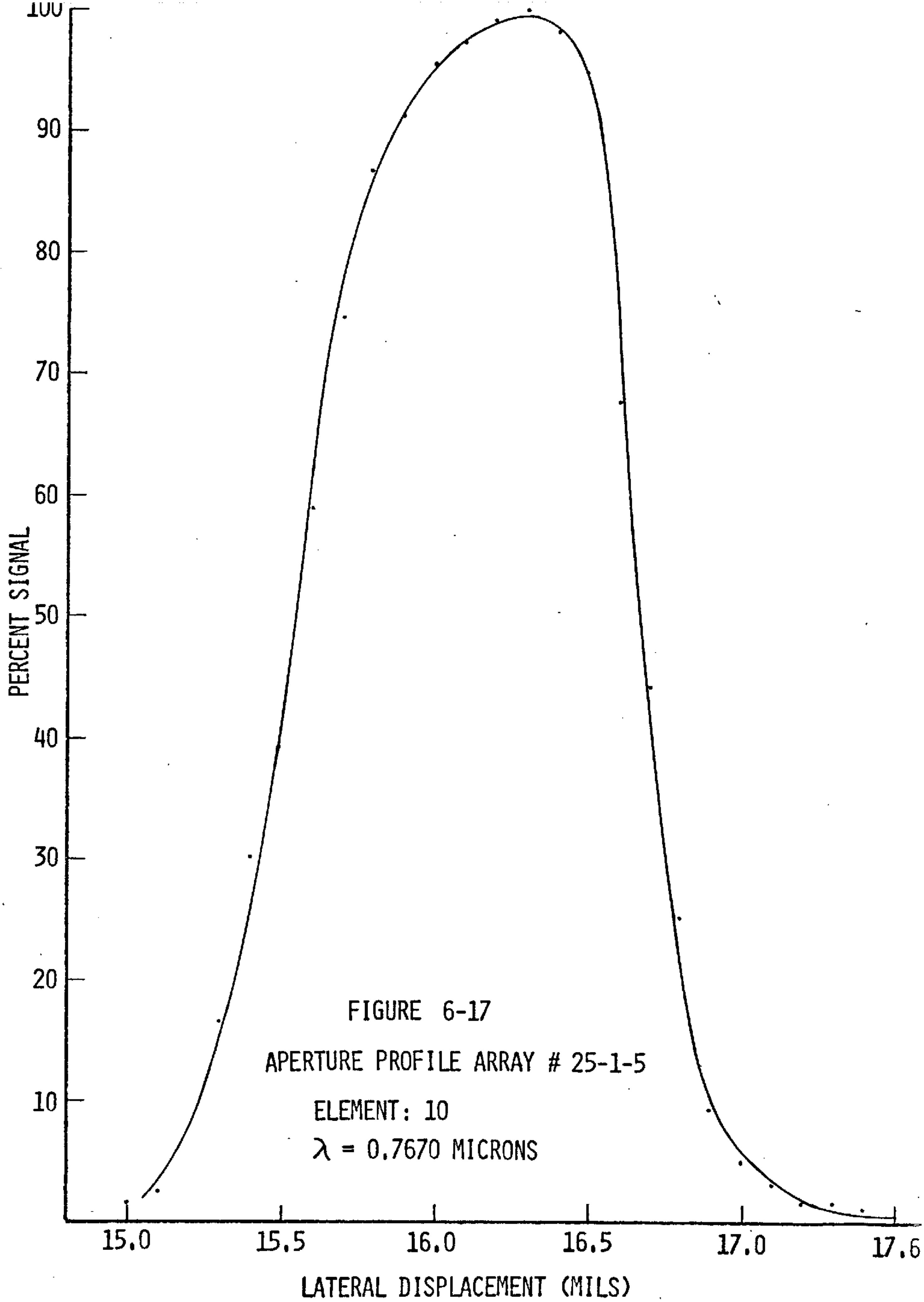


FIGURE 6-17

APERTURE PROFILE ARRAY # 25-1-5

ELEMENT: 10

λ = 0.7670 MICRONS

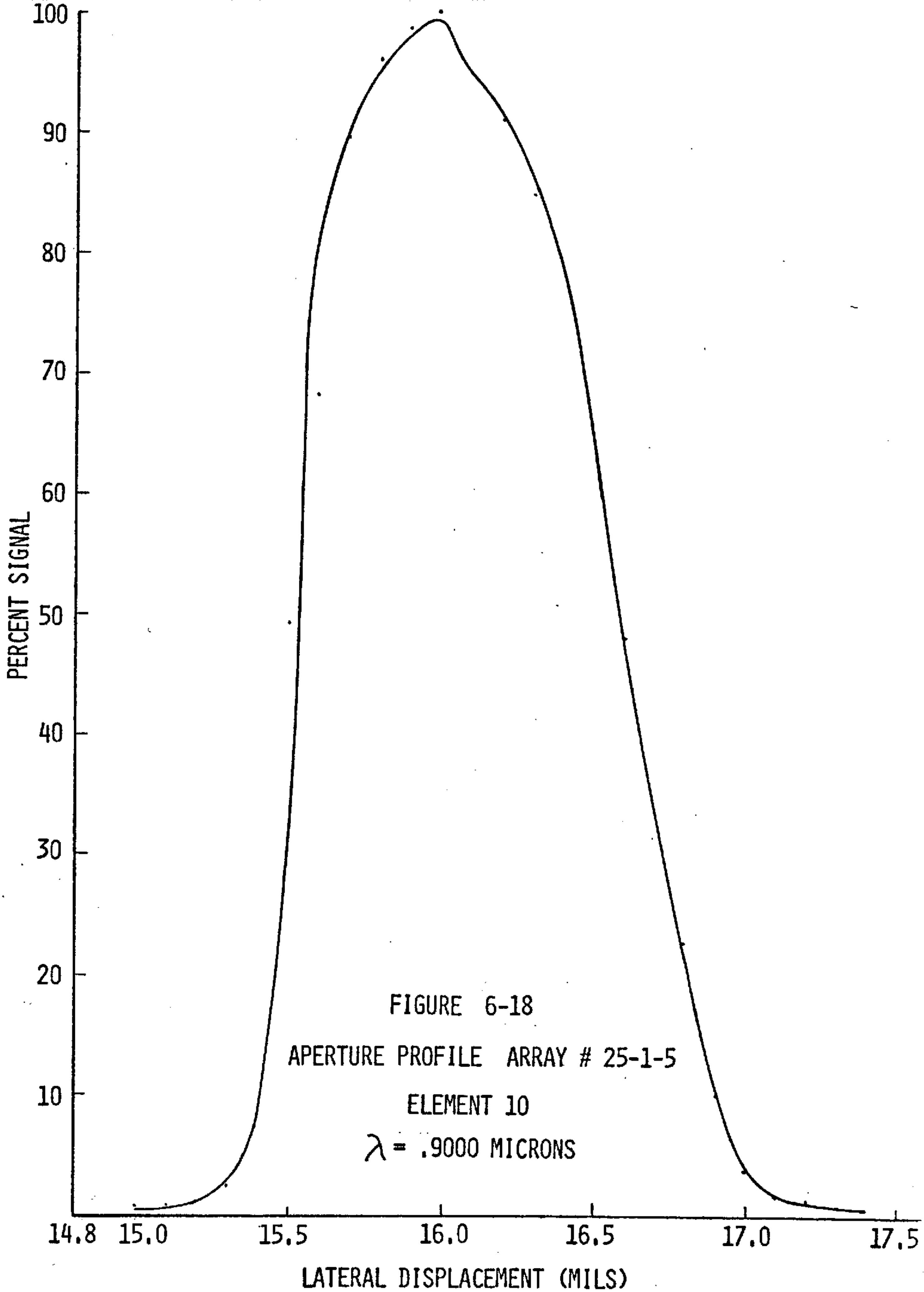


FIGURE 6-18

APERTURE PROFILE ARRAY # 25-1-5

ELEMENT 10

λ = .9000 MICRONS

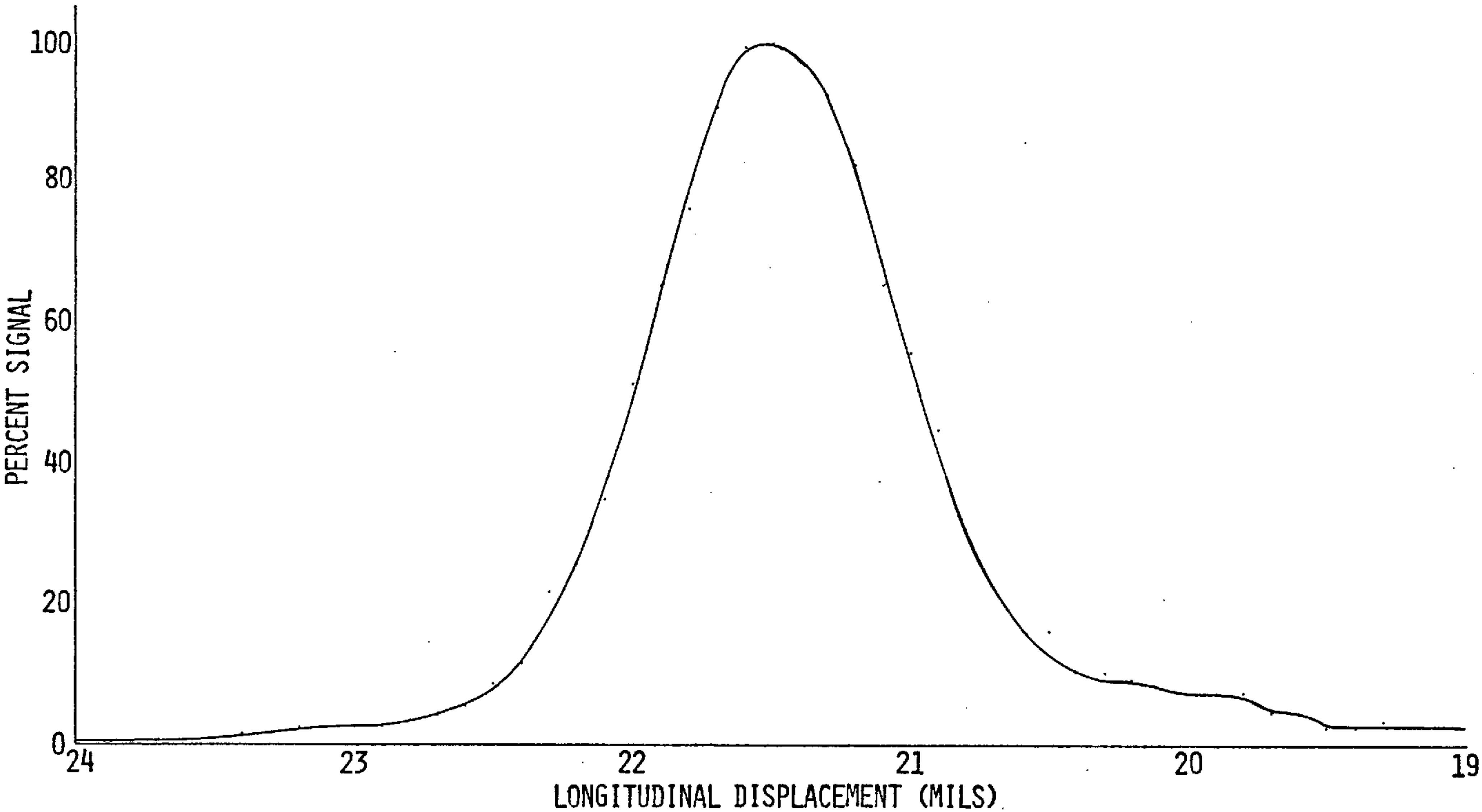


FIGURE 6-19

CROSSTALK ARRAY # 25-1-5 ELEMENTS 8 THRU 12

λ = 0.7670 MICRONS

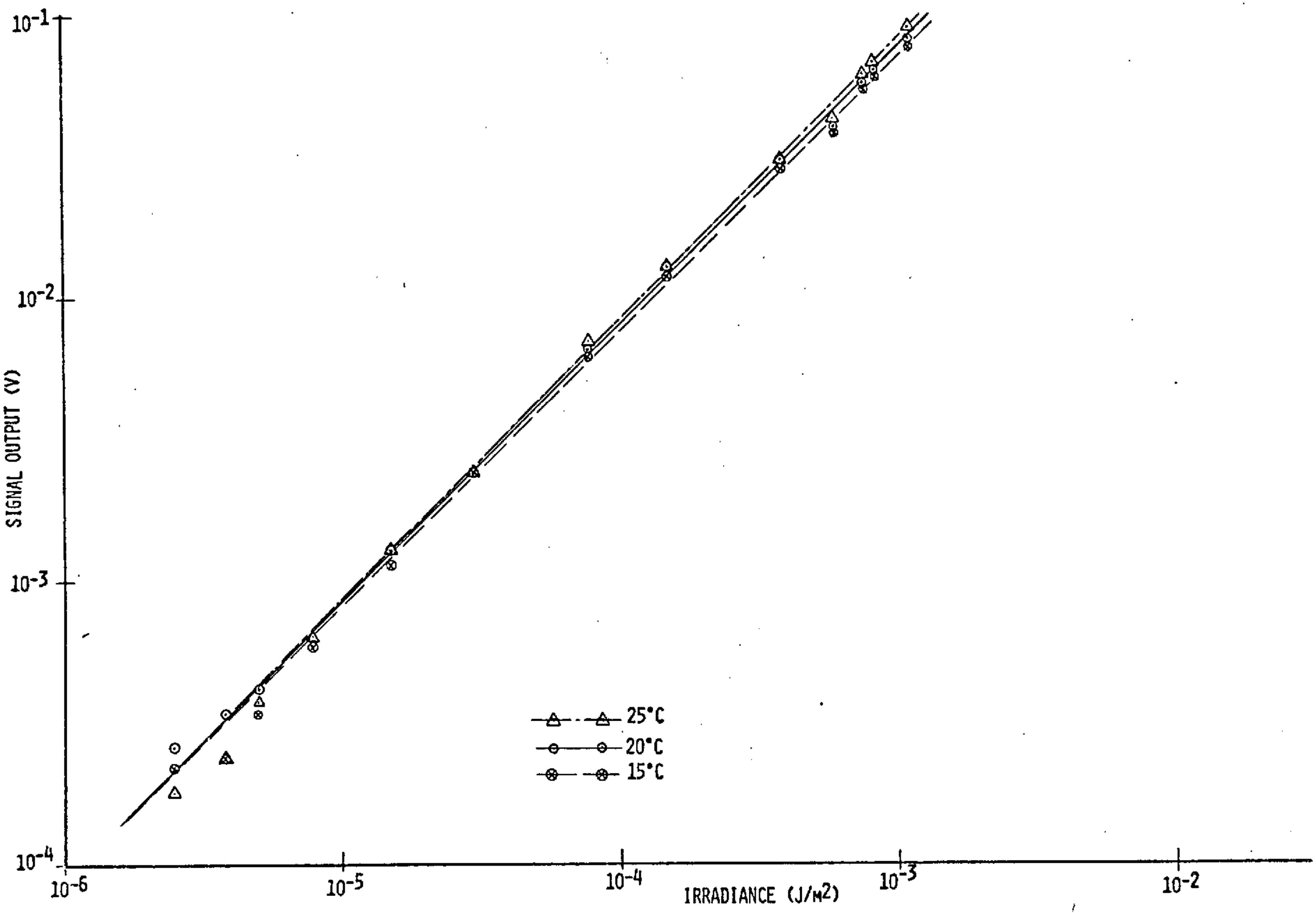


FIGURE 6-20 TEMPERATURE TEST

Table 6-4 lists the array serial number, the mean, minimum and maximum dark signal at the output of the on-chip amplifier (V_O), the array's saturation signal (V_{sat}) and the ratio of the saturation signal to dark current.

6.9 OPERATING CONDITIONS

Table 6-5 lists the operating conditions for all CCLID's tested under this program.

6.10 IMAGING EXPERIMENT

To test the imaging capability of the CCLID-500, a target was mounted on a rotating drum and imaged on the CCLID. The drum rotation simulates the motion of the vehicle, while the CCLID scanned the scene across track. The video output of the CCLID was displayed on a television monitor. Figure 6-21 shows the display resulting from a scan of a RETMA chart with a CCLID-500. Figure 6-22 shows a display of a portrait scanned by the same array.

TABLE 6-4

DARK SIGNAL

CCLID-60 S/N	DARK SIGNAL Vd (mV)			SATURATION SIGNAL V_{sat} (mV)	V_{sat}/Vd
	MEAN	MIN	MAX		
62D-1-12	2.25	2.00	2.50	487	216
62D-1-13	2.50	2.30	2.55	523	209
62D-1-16	2.00	1.75	2.25	549	275
62D-1-28	2.80	2.50	5.75	566	202
62D-1-30	2.25	2.10	2.50	584	260

TABLE 6-5

OPERATING CONDITIONS

CCLID S/N	NUMBER OF ELEMENTS	$\phi_{P1}\phi_{X1}\phi_{V1}\phi_H$ SWING (V)		ϕ_R SWING (V)		V_{OG}(V)	V_{DD}(V)	V_{DR}(V)
		LOW	HIGH	LOW	HIGH			
61A-1-16	500	0	4.0	0	5.0	1.4	15	15
61A-2X-9	500	0	4.0	0	5.0	1.4	15	15
62B-W4-18	500	-2.0	5.0	0	6.0	0	18	13
25-1-5	60	0	6.0	0	6.0	2.0	15	15
62D-1-12	60	-2.0	5.0	0	7.4	0	15	15
62D-1-13	60	-2.0	5.0	0	7.4	0	15	15
62D-1-16	60	-2.0	5.0	0	7.4	0	15	15
62D-1-28	60	-2.0	5.0	0	7.4	0	15	15
62D-1-30	60	-2.0	5.0	0	7.5	0	15	15
31-4-2	500	0	4.0	0	5.0	1.4	15	15

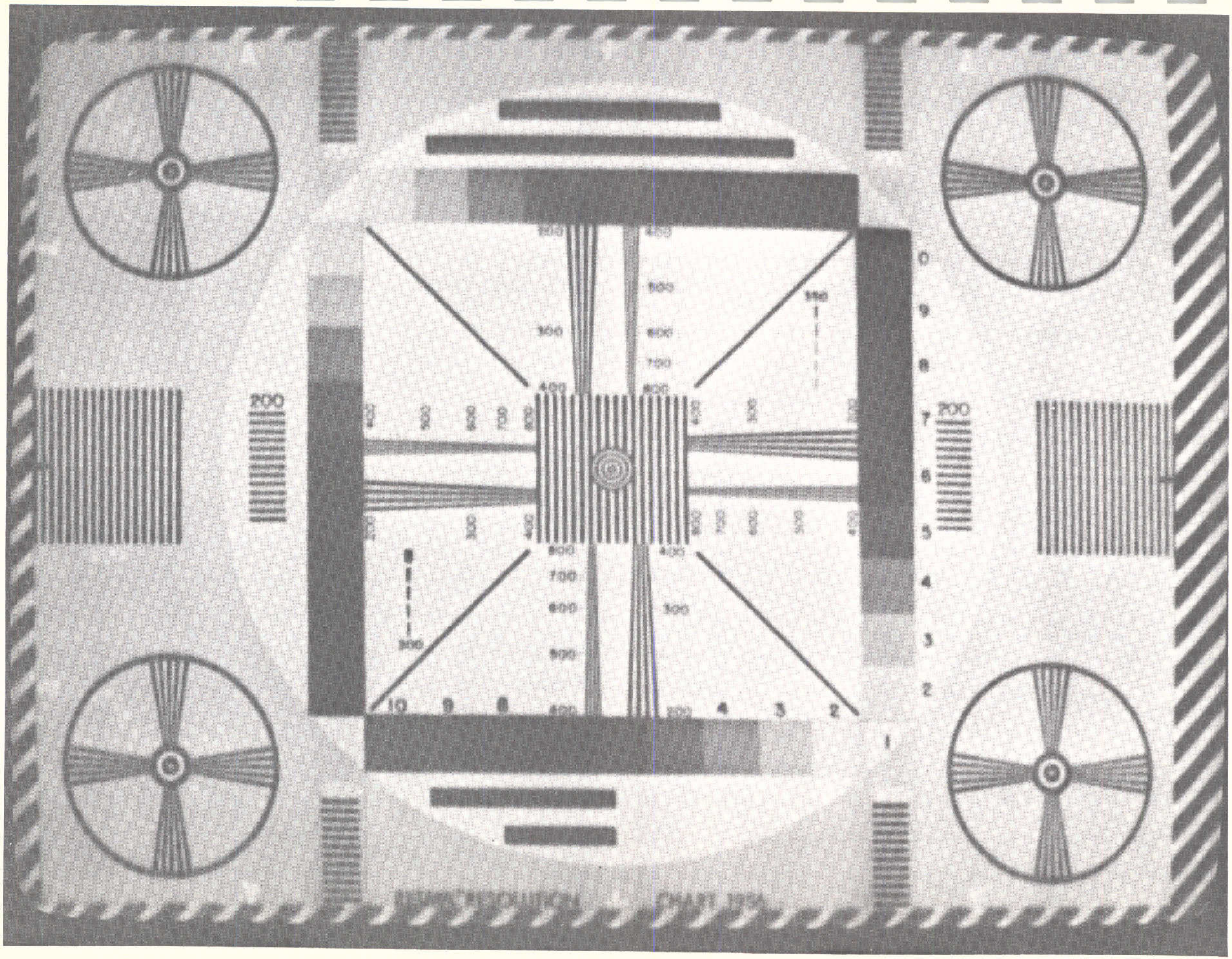


FIGURE 6-21. GRAY SCALE AND RETMA CHART
(MONITOR DISPLAY)

FIGURE 6-22. QUALITY OF SCENE (MONITOR DISPLAY)

SECTION 7

CCD DEVELOPMENTS

7.1 GENERAL

Continuing development work at FCIC since the completion of the test phase of this program resulted in device improvements as well as new devices. This section will describe the Fairchild CCD developments to date.

7.2 CHARGE DETECTION

The ultimate sensitivity of a CCD imaging device depends largely on the detection and amplification of the signal charge. The principal requirements for this output amplifier are the following: (1) the amplifier must possess sufficient gain to drive the next stage, (2) the equivalent input noise must be small enough to allow detection of the desired minimum charge at a specified signal-to-noise ratio, (3) the dynamic range must be capable of handling the largest expected input signal, (4) the frequency response must be broad enough for the intended application, and (5) the gain shape over the full dynamic range must be appropriate for system requirements.

7.2.1 Single-Ended Gated-Charge Integrator

The simplest approach to designing a detector circuit utilizes the CCD output diode itself as a gated-charge integrator, as in the CCLID 500. In this mode, the diode is charged to some fixed value of reverse voltage, V_{bias}, by a reset MOS transistor, during a time when no signal is being transferred from the register. The reset switch is then opened, allowing the output diode to function as a charge-storage detector for minority (signal charge) carriers. At the next transfer, the signal charge is stored on the diode capacitor, which results in a corresponding change in the voltage across the diode. The voltage swing is then monitored by a high input-impedance source-follower stage.

The primary purpose of the source-follower is to buffer the output diode and to provide a low impedance output capable of driving the desired load to the maximum frequency of interest.

The limitations of the simple gated-charge integrator are two-fold. First, from a practical standpoint, the output is subject to a strong component of coherent noise originating from the reset gate. This noise consists of a feed-through of the reset pulse to the output through the gate-to-source capacitance of the reset switch.

Another limitation of this technique arises from the mixing which occurs between the signal of interest and the majority carrier population of the sensing diffusion. This mixing leads to transfer noise in connection with the discharging (or resetting) of the sensing diffusion.

7.2.2 Differential Gated-Charge Integrator

The differential gated-charge integrator represents a modified version of the simpler structure with the objective of reducing coherent noise. A "dummy" diode is fabricated, identical to the signal diode in all respects except it is not connected to the CCD channel. Both diodes are connected to a common reset line through identical reset switches. A differential source-follower pair provides the final output. An external differential amplifier subtracts the major component of the reset noise from the signal.

7.2.3 Floating Gate Amplifier (FGA)

The floating gate amplifier circumvents the signal-to-noise limitations of the gated integrator structure. In operation, the charge to be sensed is brought under the floating gate by manipulation of the potentials of adjacent charge-coupling electrodes. The signal charges do not mix with other bias charges and may be moved downstream in the signal channel in the conventional CCD fashion. The same signal charges can therefore be used in successive stages of similar structure. This leads to the concept of a distributed floating gate amplifier.

The operation of the FGA depends on electrostatically coupling the signal charge to the floating gate to produce a voltage change in the floating gate potential. This change in potential is then used to modulate a channel current in a MOS. The floating gate amplifier can be designed to produce a responsivity of 60 uV/electron, with a signal handling capacity of 10^4 electrons.

A floating gate amplifier test structure developed by FCIC under Naval Research Laboratories (NRL) contract number N00014-72-C-0344 was designed to have a responsivity of 3.5 uV/electron. In testing this structure it exhibited a responsivity of 2.5 uV/electron, or approximately 5 times the responsivity of the gated charge integrator used in the CCLID 60 and 500.

7.3 LINEAR IMAGING DEVICES

Several new linear devices have been developed or are currently in development at FCIC.

7.3.1 Charge-Coupled Linear Imaging Device 500 X 1, Model B (CCLID-500B)

The CCLID-500B is a refined version of the CCLID-500. Design modifications that have been made to the old device are the following:

a) The new design has photo-elements on 0.77 mil centers. This smaller geometry implies an operating frequency as high as 10 MHz for comparable transfer efficiency, which is inversely proportional to the square of the photoelement pitch.

b) An opaque metal shield design has been provided to improve signal uniformity and to reduce odd/even dissimilarities in photosensitivity. A sink diode surrounding the entire device has also been introduced to minimize the accumulation of stray carriers.

c) An on-chip differential amplifier is employed to obtain closer temperature tracking, reduced coherent noise and improved sensitivity.

d) An aluminum buss transfer gate ($\emptyset_X$) is used for obtaining higher conductivity which results in a lower response time for this gate.

e) The incorporation of back-to-back diodes at the pulse inputs provides gate protection for longer life and greater reliability.

The mask-making process of this device has been completed; the device is being fabricated.

7.3.2 Charge-Coupled Interlaced Linear Imaging Device (CCILID)

The ILID is the most advanced linear imaging device; it incorporates element exposure control and/or anti-blooming; it possesses 0.55 mil photo-element spacings.

Features of the 255-element blooming-controlled CCILID are:

a) The analog shift register which transports the signal charge to the output is on only one side of the photogate region.

b) On the other side are a sink diode and an exposure gate. The combination of the exposure gate and sink diode provides both exposure control and/or blooming control.

c) The device has three photo-elements per shift-register bit compared to two photo-elements per shift-register bit in the CCLID-500. This requires the interlaced scanning of the photo-elements in such a way that photoelement numbers 1, 4, 7, 10 --- are scanned first; 2, 5, 8, 11 are scanned second; and 3, 6, 9, 12 --- are scanned last.

d) The output detector is the gated-charge integrator with a dummy integrator to produce the coherent noise. A differential amplifier off the chip subtracts the coherent noise from the signal output.

e) The device has a sink diode surrounding the entire device and metalized light shielding for better uniformity as in the CCLID-500B.

The blooming control and exposure control are achieved by pulsing the exposure gate for appropriate time intervals. It is also possible to achieve both blooming control and exposure control at the same time by adjusting the low voltage level of the exposure gate. In this way, the low level of the exposure gate provides for anti-blooming and the on-time of the exposure gate provides exposure control.

7.4 AREA IMAGING DEVICES

In addition to the line imaging devices, FCIC has developed charge coupled area imaging devices.

7.4.1 Charge Coupled Area Imaging Device, 100 X 100 Model A (CCAID-100A)

As its name implies, this area imager consists of 10,000 elements in a 100 X 100 format. Each cell unit consists of a sensor element and a storage/transport element. It has a 3 X 4 aspect ratio so as to be compatible with the standard television format. The cell size dimensions are 1.2 X 1.6 mil.

The CCAID operates in a two-field interlace mode compatible with standard television format. The content of all photoelements in one field is transferred in parallel into opaqued vertical transport registers. These transfer their charges, one line at a time, into the horizontal transport register which in turn feeds the video signal to a differential charge integrator serving as an on-chip amplifier. When all the data is transferred out, the second field is loaded into the registers and the transport process is repeated.

The CCAID-100A is a buried channel two phase CCD. The parallel photo transfer feature prevents smear due to charge transfers through the photoelements.

A number of developmental runs have been produced, tested and incorporated into cameras.

7.4.2 Charge Coupled Area Imaging Device, 100 X 100, Model B (CCAID-100B)

This area imaging device is currently in the design stage. A number of modifications to the Model A have been incorporated in this device.

a) The replacement of the serpentine channel stop by the comb-shaped channel stop to simplify the clocking requirements to operate the device.

b) The left-to-right inversion of the overall chip layout to conform the output to standard television sweeps, when the device is situated in a camera behind a simple inverting lens system.

c) An anti-blooming feature was added which will in general confine blooming to columns of display elements.

d) An input gate/diode structure at the end of the horizontal register is added to provide a means to conduct a routine evaluation of the transport behavior of devices without an optical input.

7.5 OTHER DEVELOPMENT

Other imaging devices in early stages of development are:

7.5.1 CCLID-1000B

A linear imaging device similar to the CCLID-500B, but with 1000 X 1 photoelements.

7.5.2 CCILID-1500

A linear imaging device similar to the CCILID-255 but with 1500 photoelements.

7.5.3 Area Imaging Devices

Several area imaging devices containing a larger number of elements than the CCAID-100 are in development.

APPENDIX A

CHARGE-COUPLED DEVICE CONCEPTS

It is already widely recognized that Charge-Coupled Device technology can create major, and revolutionary, new applications for silicon semiconductors. In memory applications there are significant advantages over existing semiconductors due to the inherent low power and the simplicity of the structure. In the field of imaging, the impact of this new technology on TV cameras can be considered analogous to that of the transistor on vacuum tubes.

Charge-Coupled Devices are a new class of semiconductor structures normally operating in (thermal) nonequilibrium and utilizing, as the signal carriers, minority charge transported by moving potential wells. In essence, therefore, a CCD is a near ideal semiconductor analog shift register. The CCD concept permits the design of highly complex devices of superior performance at potentially low cost.

Despite the fact that CCD is a new device concept, it is based on well-developed semiconductor technology which is one of its chief advantages. In addition, CCD has the attributes of:

(1) silicon fabrication simplicity
(2) high packing density
(3) high reliability
(4) low power, and
(5) intrinsic low noise analog signal processing.

Such features imply major device advantages in the areas of digital register memories and self-scanned imaging devices.

Inherently, the charge-coupled device is very simple, consisting of potential wells which are the solid-state equivalent of a vacuum, because in their ideal state there is a total absence of mobile charge carriers as long as there is not signal. It must be recognized that mixing of the charges of a particular CCD well with any other charges results in an immediate and usually large increase in the noise level above the minimum associated with dark current collection. This noise increase is irreversible and of major consequence at low signal levels. This effect is particularly important when the CCD charge is sensed by a diffusion. CCD charges must therefore remain isolated in their potential wells until their signal content has been extracted with the required signal-to-noise margin. This requirement can be met by buried channel CCD technology.

To achieve the full potential of CCD, the key elements are:

(1) A buried n-channel for high transfer efficiency, rapid charge transfer, and freedom from deleterious ion effects.

(2) The sealed conduction channel variety of silicon gate technology for high transfer efficiency, simplicity of structure, and ease of fabrication.

(3) Ion implantation to achieve and control closely the buried channel structure.

(4) Low temperature processing and multiple gettering for low, uniform, and reproducible leakage currents.

A.1 BASIC CCD OPERATION

In its original form the CCD was envisioned as merely an array of closely spaced MIS (metal-insulator-semiconductor) capacitors. Although from an operational point of view this perspective is somewhat overly-simplified, a physical understanding of the basic MIS capacitor is vital in comprehending CCD operation.

For the sake of analysis, imagine a p-type conductivity semiconductor on which there is an insulating layer and a metal electrode. If, at time $t = 0$, a positive voltage V_G with respect to the substrate is instantaneously applied to the electrode, a depletion region will be formed in the semiconductor as shown by the familiar energy band diagram in the upper portion of Figure A-1. The surface potential $\emptyset_s$ will increase to a value,

$$\emptyset_s = \frac{qN_D w^2}{2 \epsilon_s} \qquad (1)$$

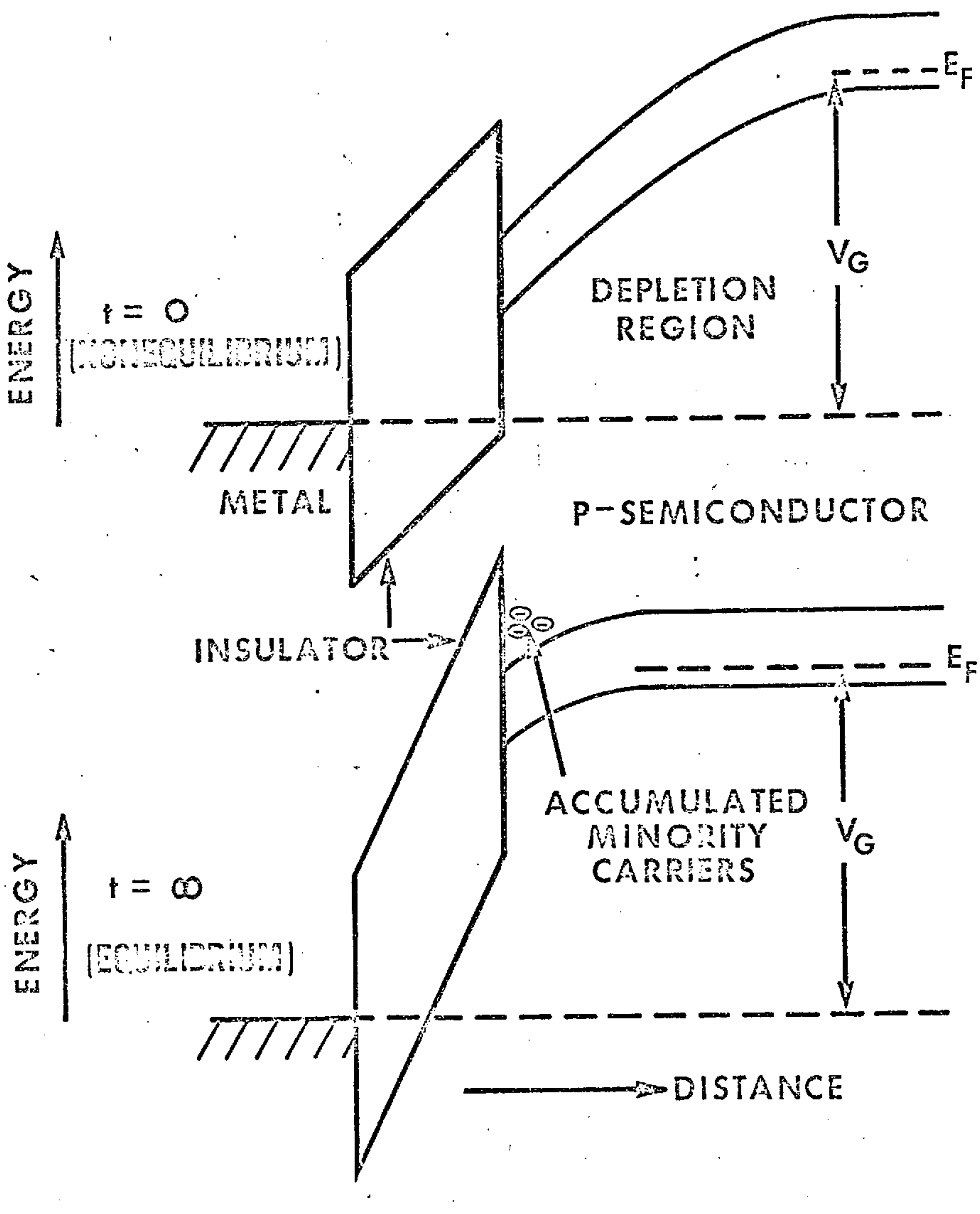


FIGURE A-1 MIS CAPACITOR

where w is the depletion depth, N_D is the acceptor doping density and ϵ_s is the semiconductor dielectric constant. The depletion depth w is dependent on the gate voltage and the device parameters. If w is eliminated from Equation (1) a relation between the gate voltage V_G and the surface potential is obtained

$$V_G = \phi_s + \frac{\sqrt{2 \epsilon_s qN_D}}{C_o} \cdot \phi_s^{1/2} \qquad (2)$$

where C_o is the oxide capacitance and the constant offset, due to work function differences and fixed ionic charge, has been ignored for clarity.

With the presence of a large depletion region, the device is not in thermal equilibrium and minority carriers (electrons in this case) will begin to accumulate at the interface between the semiconductor and the insulator. The surface potential decreases and a larger voltage appears across the insulator until equilibrium is reached (lower portion of Figure A-1). The density of electrons stored in this inversion layer is given by the equation:

$$Q = C_o (V_G - \phi_s) - \sqrt{2 \epsilon_s qN_D \phi_s} \qquad (3)$$

One inherent source of minority carriers is thermal generation. In modern, properly fabricated silicon devices, however, the thermal generation current may be so low that equilibrium is achieved only after many seconds. In such cases, the minority carriers may be introduced artificially by incident photons, surface avalanching, or a forward biased junction, and used to represent information. If this "information" can then be transferred to a detection circuit and read, the basis for a usable device is established.

A central concern in charge-coupled device design is the efficiency of charge-transfer from one electrode region to the next. Qualitatively, it can be stated that the electrode pattern must be so configured that signal carriers can move freely from one electrode region to the next when appropriate voltages are applied. An early problem in charge-coupled device performance was the ineffective coupling of charge across the inter-electrode gaps. This problem existed because the electrode pattern in the original structures was formed by etching away the metalization and thereby exposing the active oxide region. Thus, the potential in these regions was not effectively controlled by the clocking voltages and unreliable performance was characteristic of these early devices.

This problem has been eliminated by employing Fairchild silicon gate technology. With this approach, the electrode pattern is formed by selective diffusion on an undoped poly-silicon sheet. Thus the gaps are now replaced by an undoped poly-silicon film between the doped poly-silicon electrodes. This undoped region is a highly resistive dielectric and serves to define the potential in the interelectrode space and to protect the active oxide from the ambient environment. The potential is determined by the electrode voltages and the real and displacement currents within the film. Experimental results have shown that this approach is highly successful in eliminating electrostatic uncertainties associated with the interelectrode gaps.

Overall device transfer efficiency, however, is limited by surface-state trapping effects. Since the intimate juxtaposition of minority carriers with the silicon/silicon dioxide interface was an intrinisc property of the original CCD design, either surface states had to be eliminated or the basic design of the CCD's had to be altered. Pursuit of the latter alternative has led to the buried channel concept. In the conventional CCD, the basic storage element is the (MIS) capacitor normally operated in nonequilibrium (Figure A-1). The potential minimum for minority carriers exists at the silicon/insulator interface. If now an appropriate impurity distribution of polarity opposite to the substrate is introduced over a small region (approximately 0.5 um) adjacent to the surface, the potential minimum for the case of nonequilibrium will move away from the surface to a location within the impurity layer (Figure A-2). Use of this type of storage element in a CCD structure prevents contact of the signal carriers with the interface during normal operation and essentially eliminates long time-constant trapping. With this design, transfer efficiency becomes first order independent of charge level. The speed of charge transfer is enhanced, because the carriers are now further away from the electrodes and, therefore, subject to more fringing field effects, and because bulk mobility rather than the lower surface mobility applies.

A.2 CCD CONFIGURATIONS

There are several ways to configure charge couple devices so that unidirectional charge transfer is assured. Two, three and four phase designs are described in the following subsections.

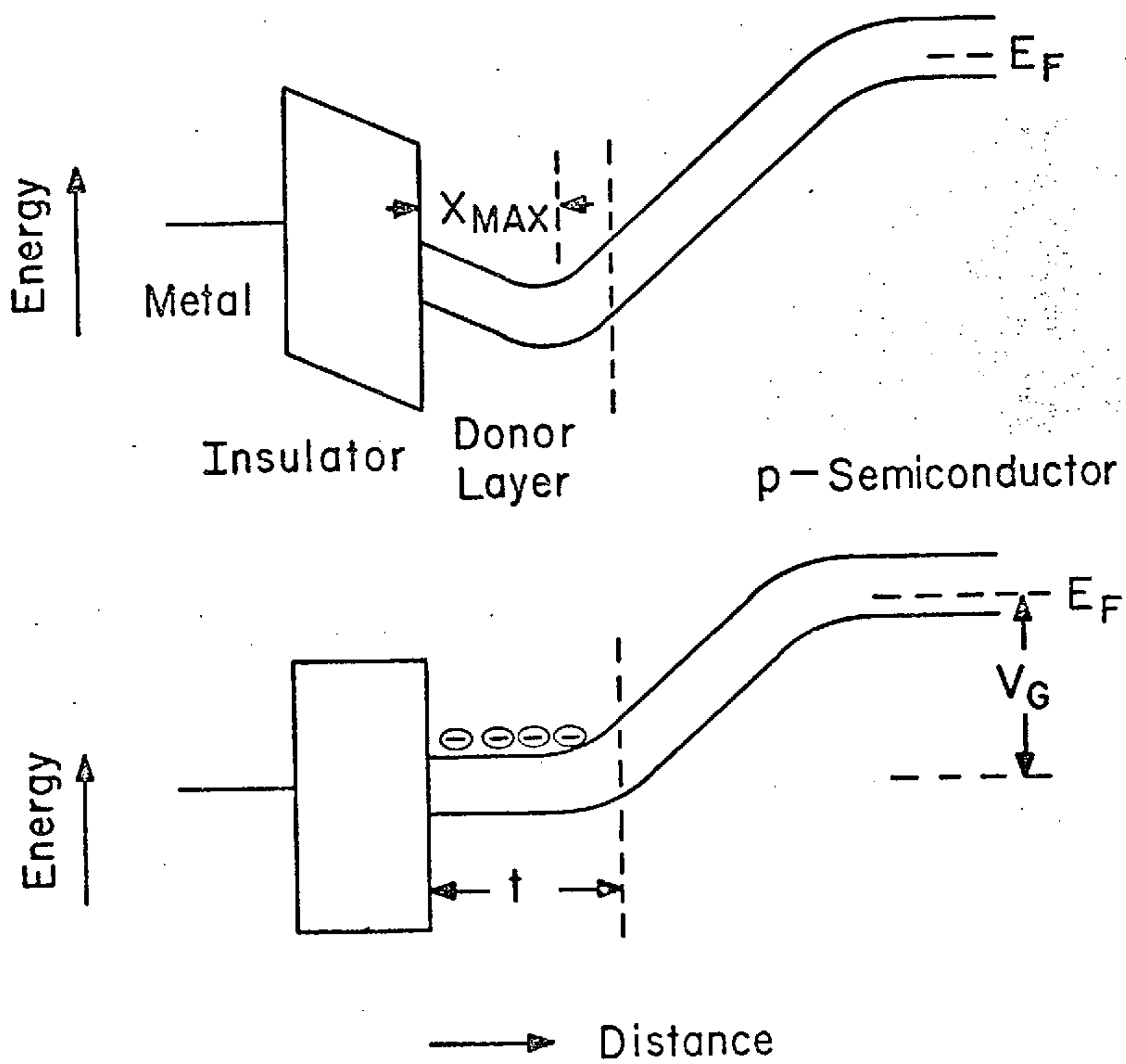


FIGURE A-2. MIS CAPACITOR WITH DONOR LAYER

A.2.1 Three Phase Unidirectional Charge Coupling

A three-phase CCD design configuration is shown in cross-section in Figure A-3. Electrode sets Ø2 and Ø3 are held at a resting voltage V_r ($V_r \gtrsim$ threshold voltage) and electrode set Ø1 is held at an applied voltage V_a ($V_a > V_r$). Any carriers present in the surface region will localize in the potential wells under the first phase electrodes. If it is desired to transfer the charge to the right, electrode set Ø2 is pulsed to a voltage V_p ($V_p > V_a$) and the potential minimum for electrons is displaced to the right. At a later time, electrode set Ø1 is reduced to the resting potential and the transfer process is completed. The electrodes of phase two are then lowered to V_a in preparation for the next transfer. In this way a device of many electrodes can be made with only three independent driving connections.

A.2.2 Two Phase/Four Phase Designs

Another configuration frequently discussed in the literature is the so-called two phase/four-phase design. This was introduced historically because of the traditional problem with etching the interelectrode gaps in the three-phase structures. It was thought, therefore, that use of the two level gate technology would eliminate the exposed gaps and produce more reliable devices. A cross-section of this configuration is shown in Figure A-4. In this figure, each gate is shown equal in size and hence charge may be stored under each gate during the transfer process. Alternatively, the upper electrodes may be made smaller and used as control gates to allow transfer between buried electrodes. The difference in oxide thickness between the even and odd phases can be used to permit a true two-phase operation. Here the upper and lower electrodes are connected in pairs. With a common voltage applied to each pair, a step in the surface potential exists due to the difference in oxide thickness resulting in an asymmetric potential well. Alternate pulsing of the two phases results in a preferred direction of charge transfer. The principle disadvantages of this structure are:

(1) dependence of the charge handling capability on the clock voltage offset, and

(2) the design does not extrapolate favorably to a buried channel configuration.

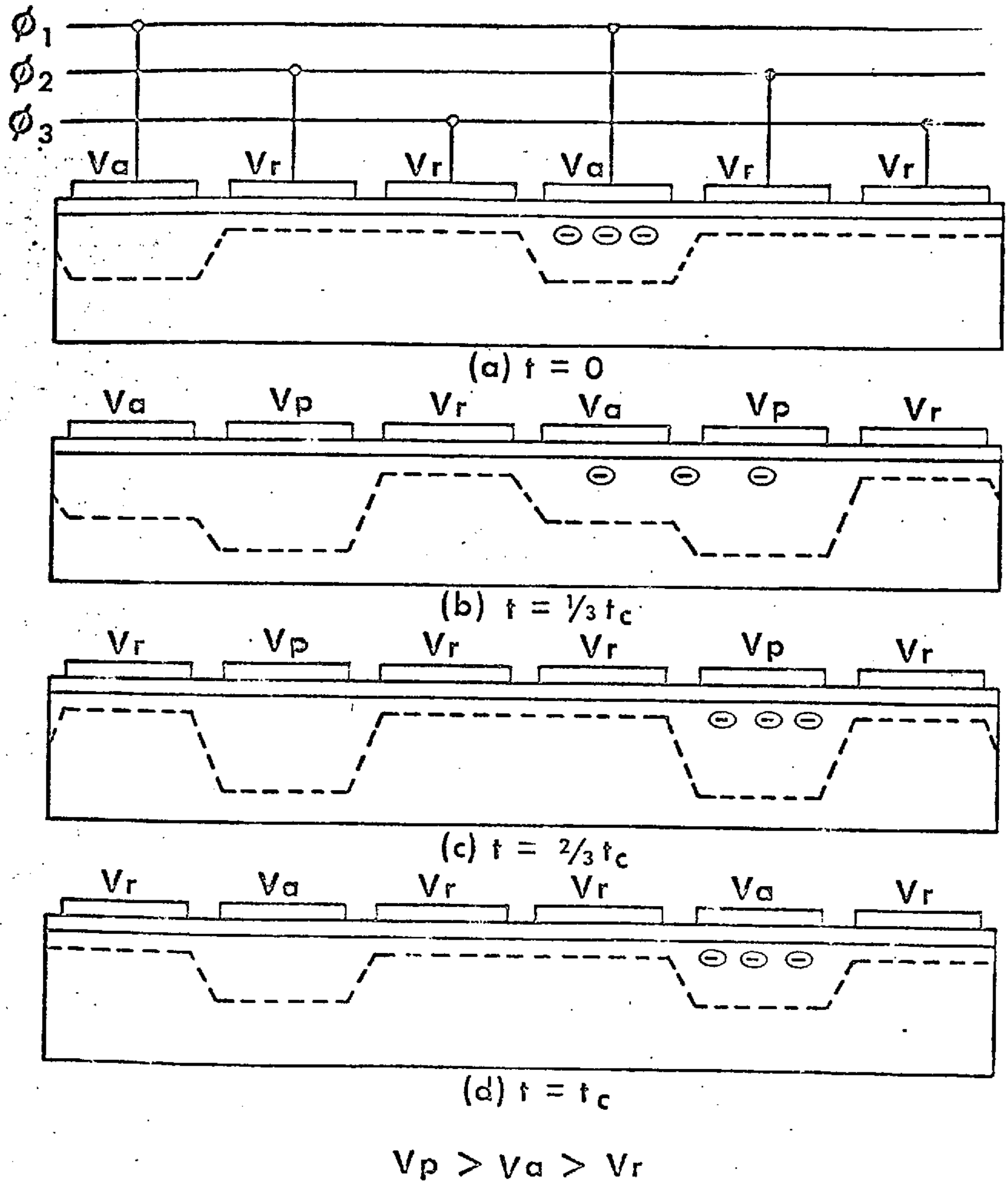
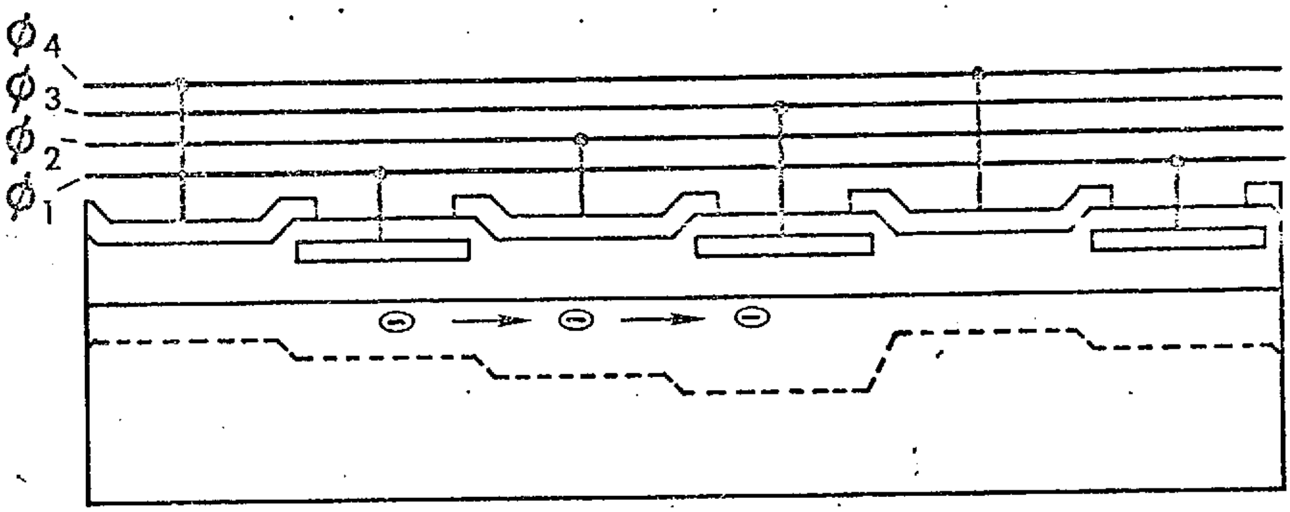
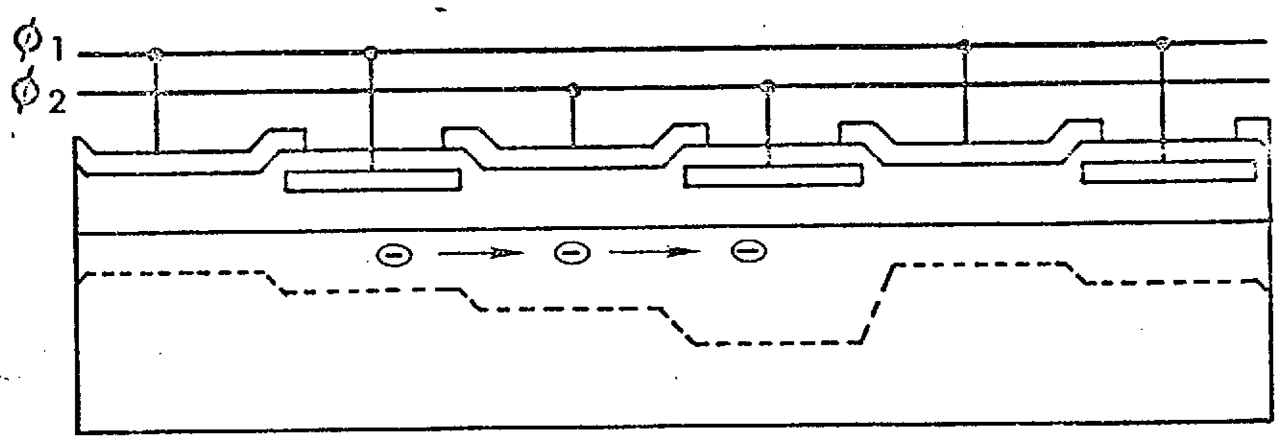


FIGURE A-3. THREE-PHASE UNIDIRECTIONAL CHARGE COUPLING



(a) FOUR PHASE



(b) TWO PHASE

FIGURE A-4. SEALED CHANNEL CCD'S

A superior two-phase arrangement which does not have these disadvantages is the implanted asymmetry charge-coupled device.

A.2.3 Two-Phase CCD With Implanted Asymmetry

The two-phase CCD with implanted asymmetry is shown schematically in Figure A-5. It has the advantages of:

(1) requiring only a single gate level when compared with a two-phase structure with stepped oxide,

(2) a uniform thickness oxide for better photolithography,

(3) compatibility with the buried channel concept,

(4) a signal-handling capability independent of driving voltage, (if the minimum necessary drive level is exceeded),

(5) simplified driving requirements.

Under each electrode of this structure is an implant asymmetrically located with respect to the center. The remaining region is implanted n^+ as in the normal buried channel configuration. If one phase is held "high" and the other "low", carriers will accumulate to the right of the "implanted barrier" under the high electrode ($t = 0$ case). To transfer charge to the right, the electrode voltage states are reversed. As the voltages on the two phases cross ($t = 0.5\ t_c$ case), carriers will not move back to the left because of the barrier. When the phases are fully reversed, however, the carriers move to the potential minimum of the next electrode ($t = t_c$ case). Thus continual out-of-phase pulsing of the two electrode sets results in carrier motion to the right. In an imaging array, a two-phase operation is a natural choice because of the compatibility with interlace scanning.

Note that it is possible to operate the two-phase CCD in a mode such that one phase is held at an intermediate D.C. potential and the other phase is pulsed around it. This suggests that a one-phase CCD is possible. Consider the structure shown in the top of Figure A-6. If the implanted donors are

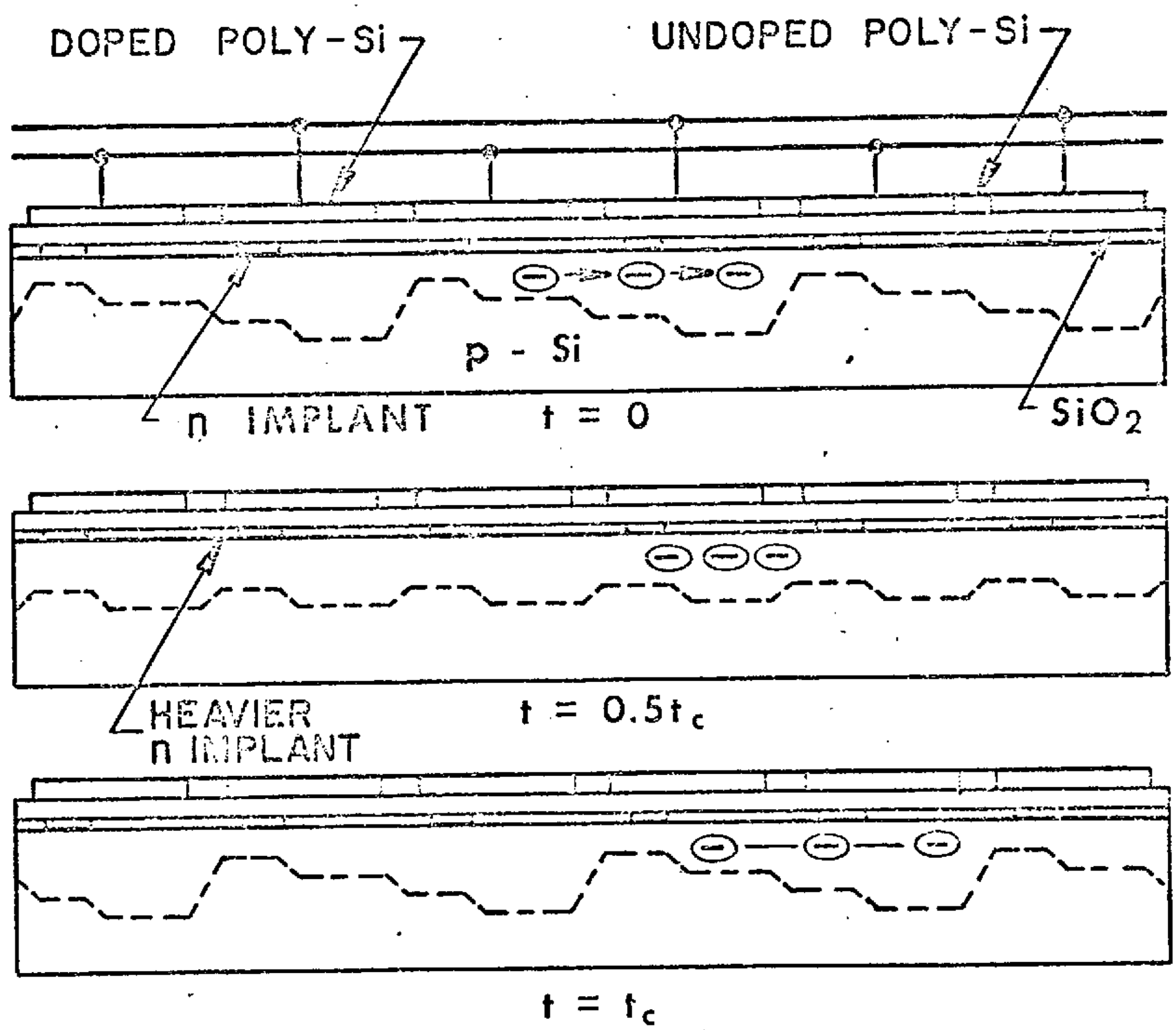
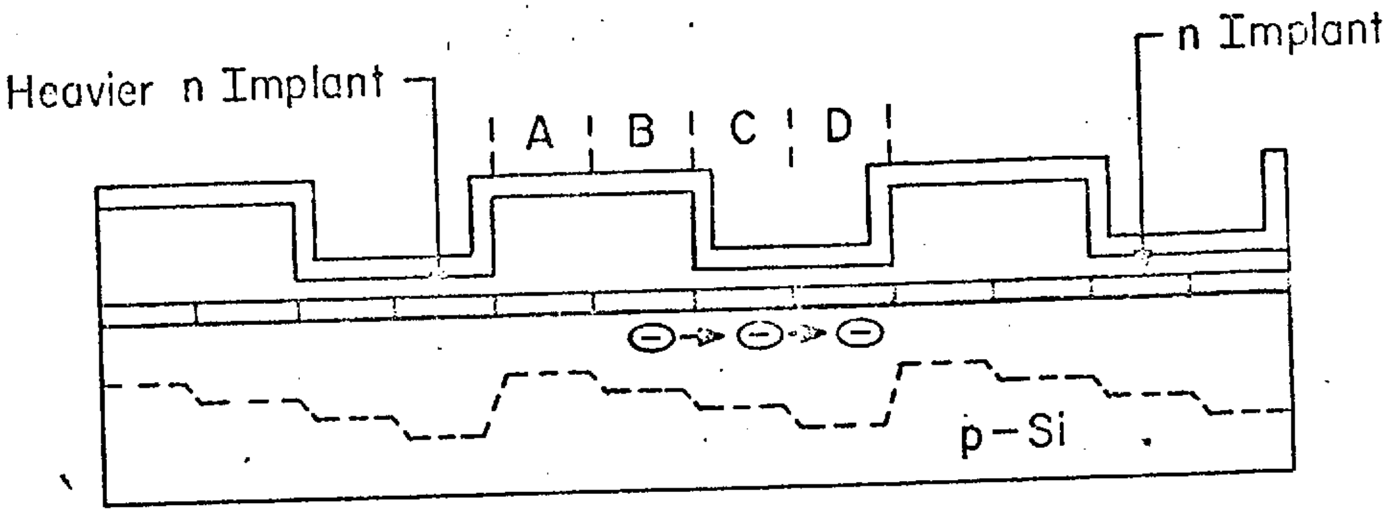
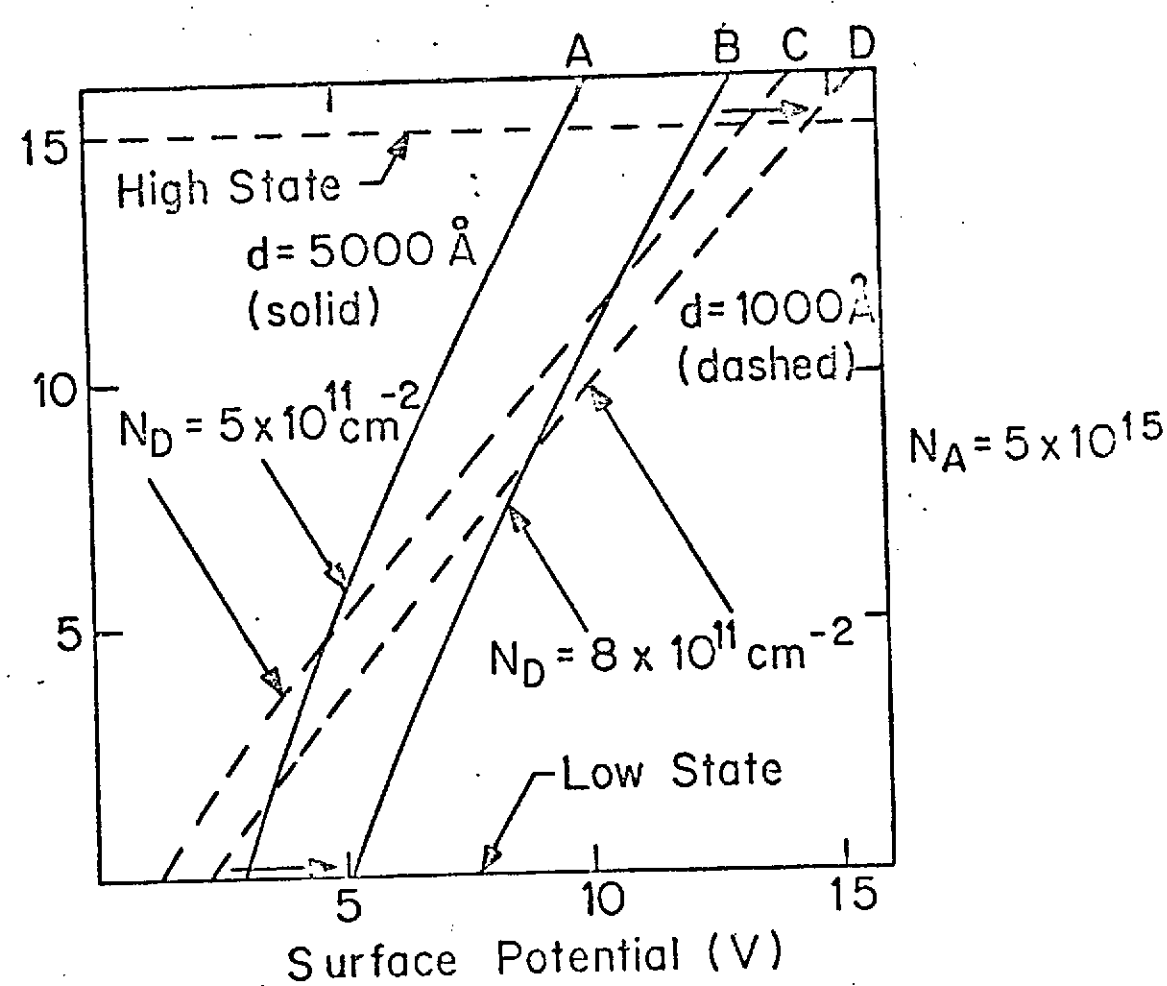


FIGURE A-5. IMPLANTED ASYMMETRY TWO-PHASE CCD



(a) Depletion region when electrode voltage high



(b) Electrode voltage - Surface potential dependence

FIGURE A-6. CURVES FOR REPRESENTATIVE DEVICE PARAMETERS, SEALED CHANNEL UNIPHASE CCD stripped of their electrons, a depletion region will form along the surface with the channel potential in the thick oxide region coming to a value heavily dependent on the implant levels but only weakly depending on the electrode voltage. The channel potential under the thick oxide may therefore be regarded as fixed. If the implant levels are suitably chosen, the channel potential under the thin oxide will swing above and below the channel potential under the thick oxide and the charge will transfer to the right just as in the two-phase device. Clocking requirements for the uniphase CCD is almost trivial because there is only one clock. The only requirement will be that proper levels for "high" and "low" states are achieved and that cycle times exceed the minimums required for the design charge transfer efficiency for the device geometry.

The relaxed clocking requirements for the implanted two-phase CCD in terms of overlapping and wave shape cannot be overemphasized. This is particularly so for high frequency operations.

The signal handling capability of a CCD is determined by the barrier height and the area of the gate. For a 3-phase structure, the barrier height is controllable externally by changing the high and the low levels of the clocks. For two-phase and uniphase structures, the barrier height is determined by the implantation levels. Therefore, the output saturation signal is insensitive to the clock voltages for two-phase and uniphase devices. A design level of about 5 volts provides good signal levels and is consistent with reasonable drive voltages.

A.3 SUMMARY

The charge-coupled device is a nonequilibrium, minority-carrier structure characterized by low power, low noise and simplicity of design. When configured using the Fairchild silicon gate technology and the buried channel concept, the devices are also efficient, reliable and stable.